a LIGHTWAVE®

LiveWebcast

Streamlining Photonic Integrated Circuit Development

September 15, 2015

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Streamlining Photonic Integrated Circuit Development

LightWave Webinar

Sep. 15, 2015

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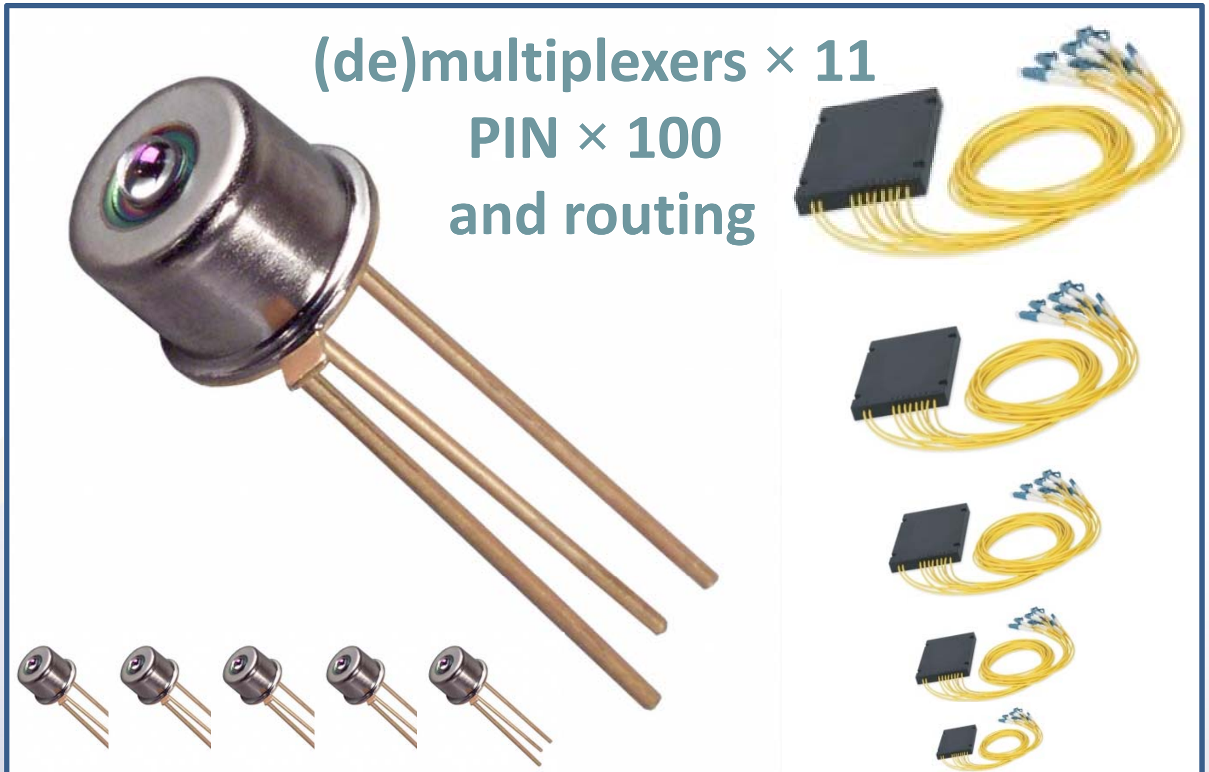
Sponsoring PIC Service Providers

- Foundries
  - Silicon Photonics
  - TriPleX
- Design software
- Packaging
- Turn key design houses
- Organizer

Agenda for This Presentation

- Why are PICs gaining momentum?
  - 100G coherent and 100G datacom are leading the way
  - But other areas are picking up (sensing, lifesciences, military…)
- Introduction to foundry services
  - Generic processes
  - Pros & cons of MPWs
- Design software
  - Electronic and Photonic Design Automation (EDA & PDA)
  - Specific attention to PDK (process design kit)
- Overview of packaging services
- Benefits of using a turn-key PIC design house

What Is a Photonic IC?



Single Photonic Integrated Circuit

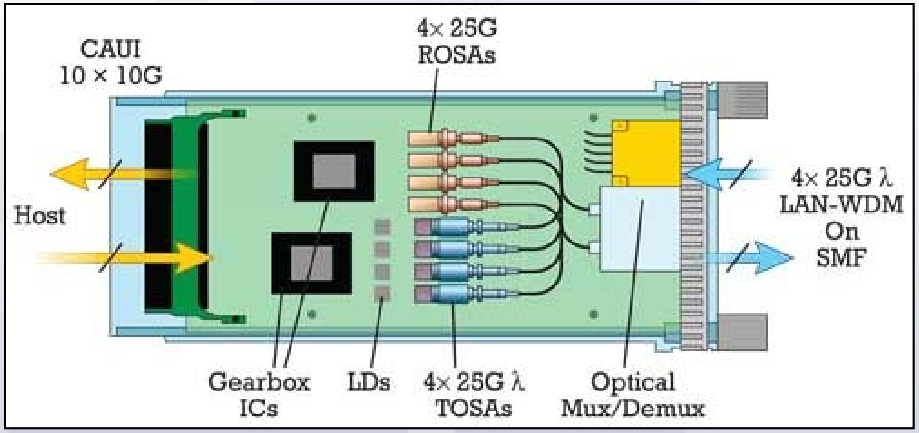
6 mm × 8 mm FBG sensor unit

- A PIC combines several components within a single chip
- Benefits are smaller size, lower cost, better manufacturability
- Some of the cons can be compromises in performance and/or yield

Why Are PICs Gaining Momentum?

- In the past, most of fiberoptics consisted of a LD, a fiber, and a PD
  - So there simply was little that could be integrated

- WDM did not help because transmit lasers were all on different linecards
- But 100G telecom/datacom have completely changed the situation
  - Now there is plenty optics in a small module & size constraints require integration



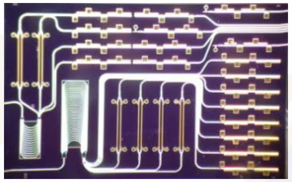
Source: Jon Anderson (Opnext) , Nov.1, 2011 Lightwave

- Demand for PICs is now also increasing in sensing, life sciences, military,…

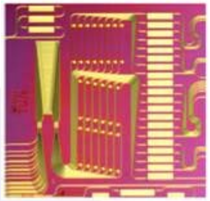
If You Need a PIC, Where Do You Go?

- You need an application specific PIC

Fiber to the Home
Wireless



Medical
Bio-imaging

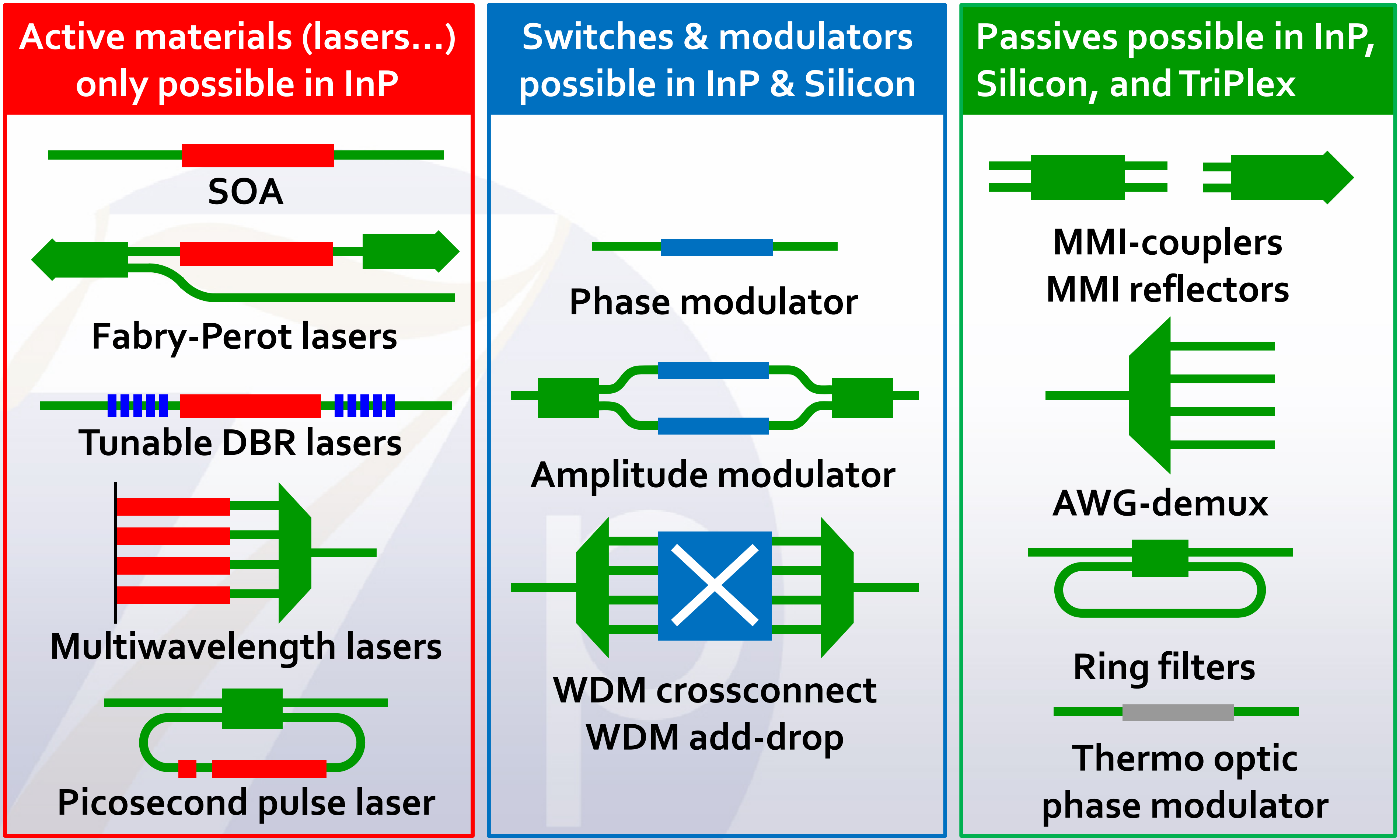


Datacom
Switching

Sensor
Readouts

  - Please note that electronic ICs have paved the road for 50 years
- You need to decide on <u>material</u> and <u>foundry</u>
  - Options: InP, Silicon, or TriPleX (excluding PLC and $LiNbO_3$)
- Also need to decide on <u>MPW vs. a custom run</u>
  - MPW reduces costs, but custom runs may be needed in the end anyway (for volume and/or for unique performance)

Decide on a Material: InP, Si, TriPleX



Comparing MPW offers in InP, Si, TriPleX

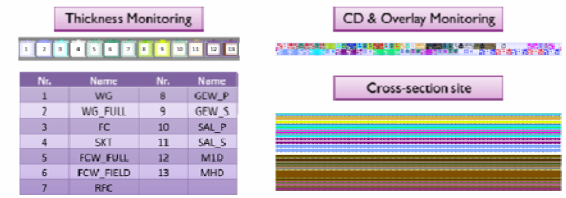
Broker	Process	Lasers	SOAs	TDBR	Modulators / Phase shifters				Detectors			Prop loss
					L (mm)	Vp - Pp	Loss (dB)	B (GHz)	R(A/W)	B (GHz)	I_{dark} (nA)	dB/cm
JePPIX	Oclaro TxRx 10G	YES	YES	YES	1	3.5	< 2	> 10	0.8	10		2-3
JePPIX	HHI TxRx 25G	YES	YES	YES	0.5	(25 mW)	< 2	(kHz)	0.8	40	< 10	1-2
JePPIX	SMART TxRx 10G	YES	YES		2	7	< 2	10	0.8	10	< 20	3-4
JePPIX	TriPleX (DS-500-170)				1-2	(500 mW)	< 0.1	(kHz)				< 0.5
	VTT 3 µm SOI				1		< 0.1	(kHz)				0.1-0.15
Europractice	Imec ISIPP25G+				1.5	7	6	20	0.5	> 50	< 50	1.5-2.5
					0.04*	2*	5*	>50*				
Europractice /LETI	CEA-LETI Si310-PHMP2M NEW!				1 - 4	< 7.5	<2.5	< 12	0.7	30	< 10	< 2.5

*) Ge EA Modulator

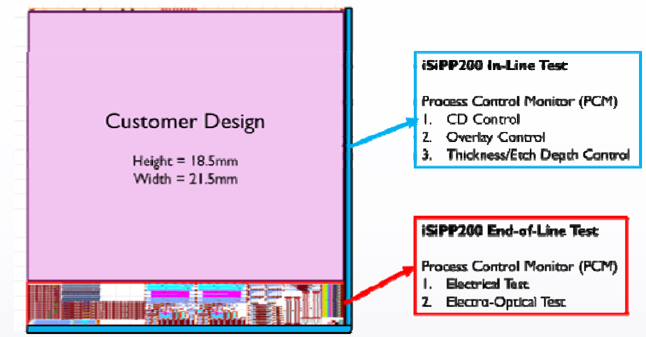
- TriPleX & VTT 3 µm SOI lowest losses. TriPleX suitable for visible light
- For active components with gain, only InP can be used
- E.g. for modulators & detectors, InP and Silicon have comparable performance
- Silicon is key for high integration density, reproducibility, and volume scalability

Material: Key Drivers Behind Silicon

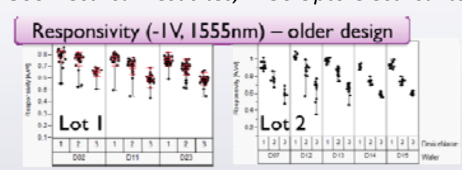
- Process maturity
  - CMOS fab-based processing
  - Fidelity-Uniformity-Reproducibility-Scalability
  - Compatibility with 3D process integration
  - Laser integration compatible on 200mm CMOS foundry
- Extreme integration density
  - WG width (450 nm), Bend radius (2-3um)
  - 16 channel AWG (300umX300um)
- High speed modulators
  - Traveling Wave, Ring modulators, Ge EAM (50G)
  - Small footprint (ring modulators)
- Photodiodes
  - ~1A/W responsivity, and very low dark current
- Automated Testing
  - In-line process parameter trend-charts
  - Wafer-scale end-of-line functional testing
- PDK and Library Maturity
  - Mature and proven design tools and flow
  - Vast number of tested C and O band components
  - Device models for library components

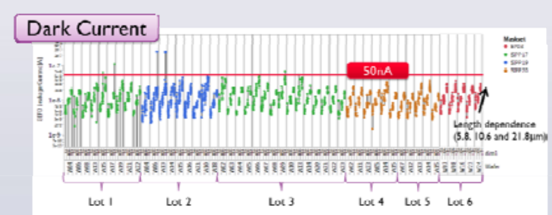


*Automated tracking of **132** in-line process parameters (scatterometry, TDSEM, In-lineFIB, ellipsometry etc.)*



*End-of-line wafer scale testing. Standard test-suite. **>500** Electrical Test sites, **>150** Opto-electrical test sites*

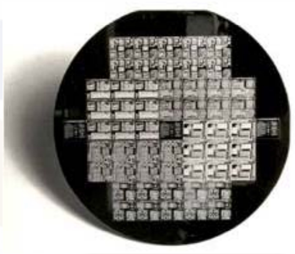




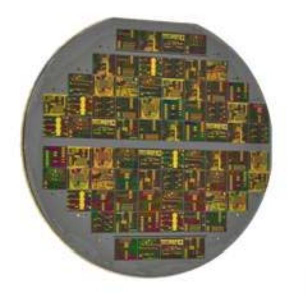
Lot to lot photodiode variations

Deciding on MPW vs. Custom Runs…

- Multi Project Wafer (MPW) shares cost between users



MOSIS started MPW in Electronics ICs in 1981



Photonics MPW now by JePPIX, EUROPRACTICE, LioniX, and MOSIS

  - Lower cost is ideal for prototyping
  - MPW broker provides complete ecosystem
  - MPW uses a generic platform
- Custom runs may be beneficial in volume
  - Can run more frequently
  - Can optimize process for better yield or unique performance

MPW vs. Custom: Generic Processes

- MPW users all share the same generic process
  - Imposes limits, but comes with a library of building blocks
  - “Lego” building blocks allow for virtually all chips
  - >350 PICs developed in generic fabs via MPW runs

- There are several key MPW brokers:
  - Europractice-IC for Silicon photonics
  - LioniX for TriPleX material (Si_3N_4/SiO_2)
  - JePPIX for InP: Smart Photonics , Oclaro, and HHI
  - AIM Photonics won the IP-IMI award in US, being formed
  - Each MPW broker brings its own solution ecosystem

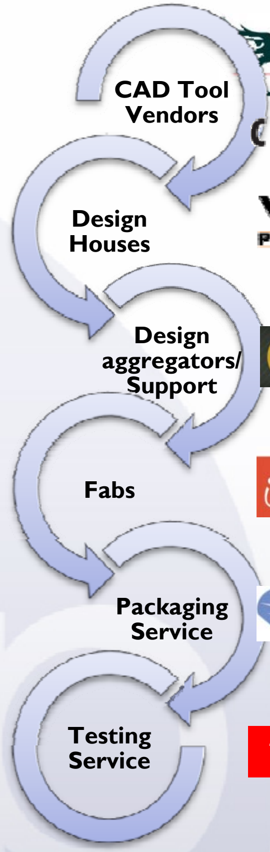
List of Brokers for MPW foundries

Technology	Broker	Runs/Year
Silicon Photonics		
Imec PSV	Europractice/MOSIS	2
Imec ISIPP25G+	Europractice/MOSIS	3
CEA-LETI Si310-PH	Europractice	1
CEA-LETI Full Platform SI310-PHMP2M	CEA-LETI	2 (starting 2016)
IHP PIC	Europractice	1
VTT	VTT	1
IME Full platform	IME	3
Indium Phosphide		
SMART Photonics	JePPIX	3..4
Oclaro	JePPIX	1
Fraunhofer HHI	JePPIX	2
Silicon Nitride		
LioniX	LioniX / JePPIX	3..4

Brokers: Introducing Europractice

EUROPRACTICE IC SERVICE

Key Features	Value Chain	Actors
Design Flow Tech Support	CAD Tool Vendors	PhoeniX Software, Mentor Graphics, Synopsys, cadence, LUCEDA Photonics
IP Blocks System Design	Design Houses	VLC Photonics, Bright Photonics
New users Localized Support	Design aggregators/ Support	The MOSIS Service, ePIXfab, CMC Microsystems, 博微
PDK Quality TAT	Fabs	ihp, cea leti, imec
Custom / Standardized	Packaging Service	Tyndall National Institute
	Testing Service	TBD



- Europractice completed 545 designs using 10 technology nodes in 2014
- Europractice brokers MPW runs for IMEC, LETI, and IHP

Si Photonics MPW Foundries

Technology	IHP	Imec	LETI NEW!	VTT
SOI Type	SOI 220nm/2µm BOX	SOI 220nm/2µm BOX	SOI 310nm/800nm BOX	SOI 3µm/3µm BOX
Access	Europractice	Europractice/MOSIS	Europractice/LETI	VTT
Passive SOI etching steps	2	3+1poly	3	3
PDK Tools	IPKISS/TexEda/ (PhoeniX Software)	Mentor Graphics/ Synopsys/IPKISS/ PhoeniX Software	Cadence/ PhoeniX Software/ Mentor Graphics	PhoeniX Software
Min Critical Dimension on Mask	130nm	130nm	120nm*****	600nm
Minimum Cost Euro/mm²	180**	278** / 1508****	124** / 935***	120**/ 250***
Polarization Dependence	TE only	TE only	TE only	Low
Packaging	Tyndall Institute	Tyndall Institute	Tyndall Institute	VTT
Passives Building blocks	x	x	x	x
Active Building blocks	x	x	x	Thermo optical
Minimum number of Die	25	25	15*	1 large or 8 small
Low volume production	x	x	x	x

Notes:
*) Mini block available for academic
**) Cost for passive only
***) Cost for Heater technology
****) Cost for active
*****) Compatible design rules with 300 mm industrial foundry

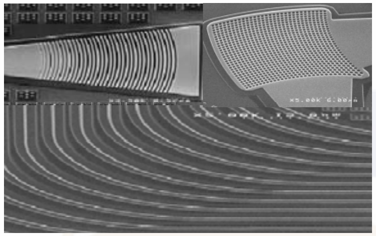
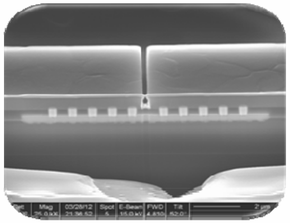
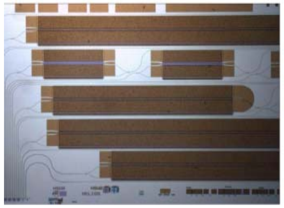
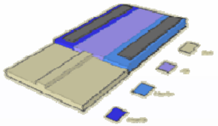
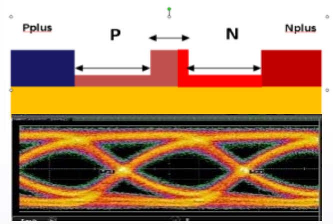
FROM RESEARCH TO INDUSTRY

cea tech

λ=1.31 µm TE mode

Global LETI MPW offer on 310nm Si / 800 nm BOX on 200mm platform

leti

Passives components	Heaters	Lateral Ge PIN diode	Carrier depletion PN MZ Modulator
 +	 +	 +	
Coupler 1D **IL < -2.5 dB loss** ***Coupler 2D*** **IL < -4,5 dB loss** **Si310-PH** *Monomode Rib waveguide :* ➢ ***propagation losses: < 2.5dB/cm*** *Multimode Rib Waveguide:* ➢ ***propagation losses: < 0.3dB/cm***	➢ Thermal efficiency: 0,5 > TE >0,2 nm/mW Sheet resistance: 5,5 ohm / Sq	 ➢ **Responsivity: > 0.7A/W** ➢ **Dark current: < 10nA @ -1 V** ➢ **Bandwith -3dB in S21 @ -1V : 30 GHz**	 ➢ **Vpi.Lpi < 2,5 V.cm** ➢ **Prop Loss < 2 dB/mm** ➢ **Data Rate up to 25Gbps**

Sign in Q1 or Q4 2016 through Europractice IC

Si310-PHMP2M sign in 2016

- ❑ Very high performance building blocks for λ=1.31 µm and λ=1.55 µm
- ❑ Compatible Photonics and process 3D from CEA-LETI for Electronics integration
- ❑ PDKs available via Cadence, Phoenix software, and Mentor Graphics
- ❑ Technology compatible design rules with **300 mm industrial foundry**

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NEW SOI PLATFORM!

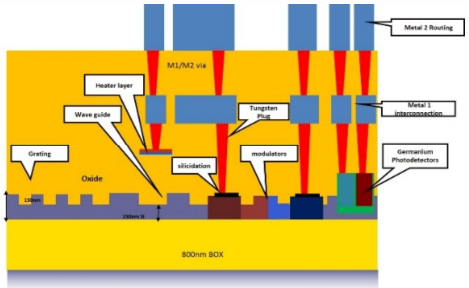
Silicon Photonics

λ=1.55 µm
λ=1.31 µm
TE mode

NEW SOI PLATFORM!

- SOI substrate High Resistivity: BOX 800nm / Si 310 nm
- Passive structures (3 mask layers DUV 193nm)
  - min CD 120nm
  - 300nm /150nm
  - 150nm /0
  - Optional Slab 65nm
- Germanium PD's fabrication
  - n and p implant level
- Heater layer (Optional)
- MZ and RR Modulators
  - (2 n level and 2 p level implants)
  - Silicidation
- Tungsten Plugs for interconnection
- 2 level of AlCu Metallization for routing

Compatible with LETI_3D integration

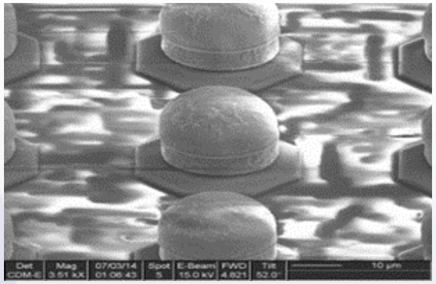


Full platform

MPW offer

available from 2016

+

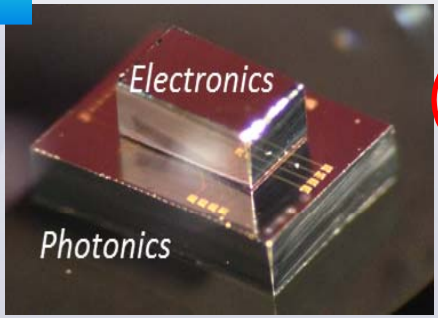


CEA –LETI 3D

MPW offer via CMP Broker

available

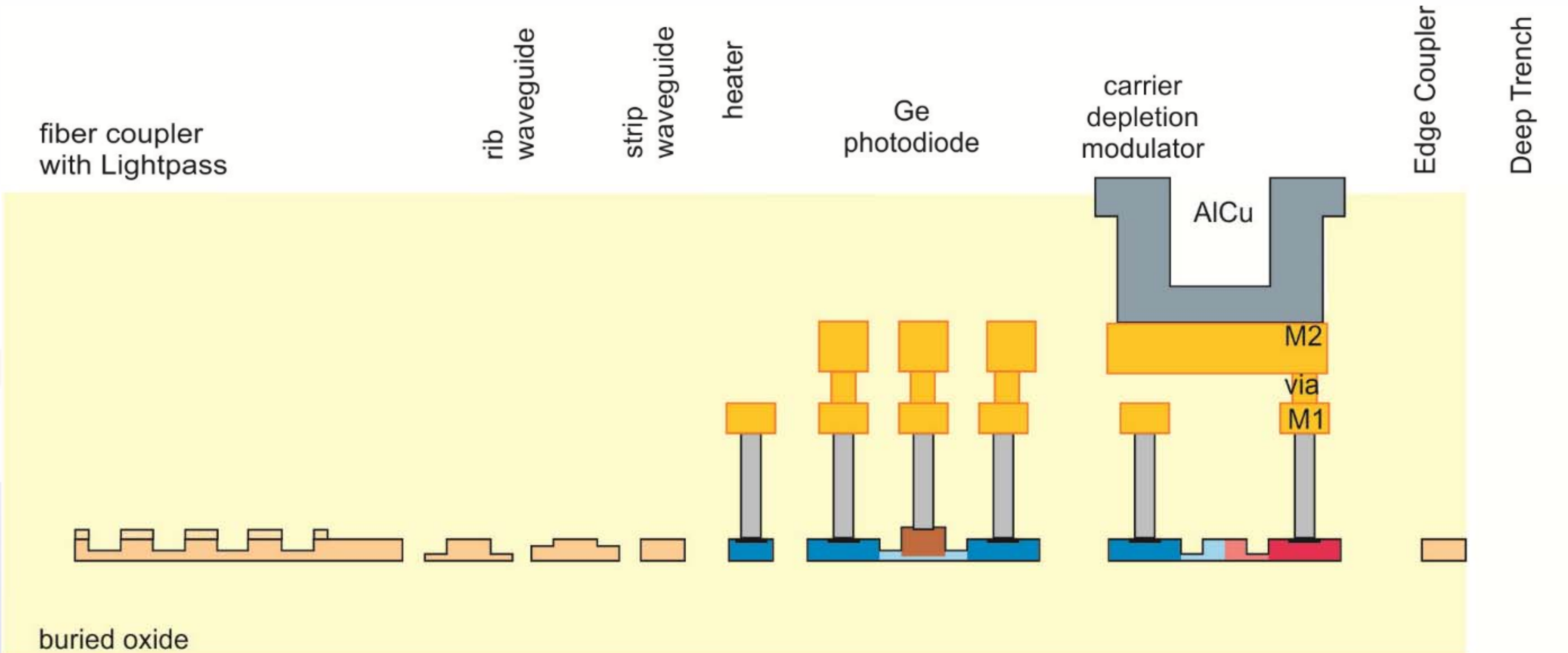
=



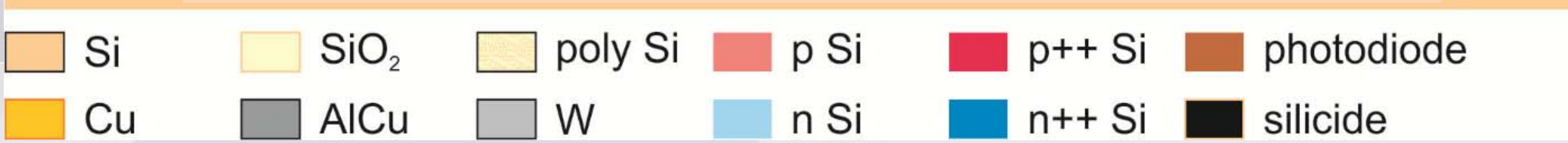
Photonics and electronics integration

available from 2016

Silicon Photonics Platform ISIPP25G+

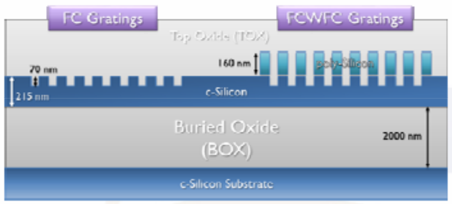


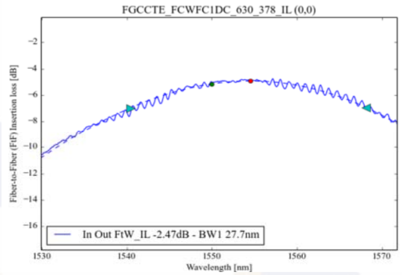
- 200mm Photonics SOI wafers with 220nm top Si and 2um BOX
- Processes based on 130nm CMOS toolset plus
  - 193nm lithography for all silicon waveguide patterning steps
  - 3n/3p level implants for plasma dispersion modulators
  - 2 level metallization
  - Edge Couplers
  - Selective Ge epi for waveguide-based photo-detectors and F-K modulators
- 24 mask layer process



ISIPP25G+ Performance: Passives

TE Grating Couplers

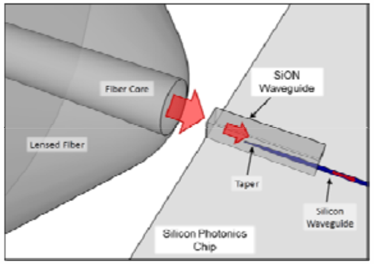


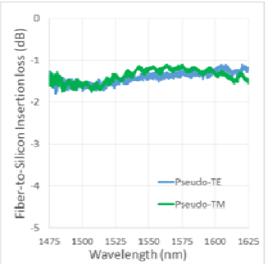


- Fiber-to-waveguide IL ~2.5dB (SMF, no IMF)
- Peak WL control within-wafer 1-σ <4.0nm
- 1dB Bandwidth ~29nm (no IMF)

Note: data is based on multiple wafers / multiple lots

TE/TM Edge Couplers



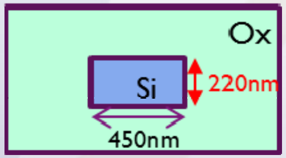


- Fiber-to-waveguide IL <2dB (High-NA, IMF)
- Polarization dependent loss <0.5dB
- 1dB Bandwidth >100nm

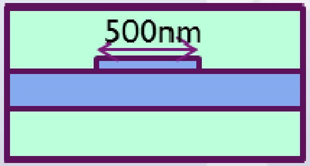
Note: O-band designs in development

Waveguide Loss

SWG-WG



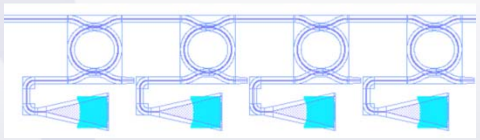
RWG-FC

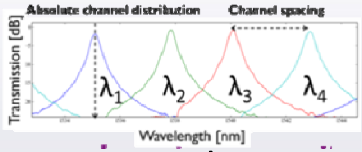


- SWG-WG < 2.0dB/cm
- RWG-FC < 1.0dB/cm

Note: data is based on multiple wafers / multiple lots

Waveguide-based filters



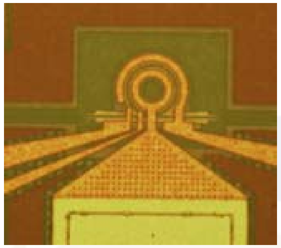


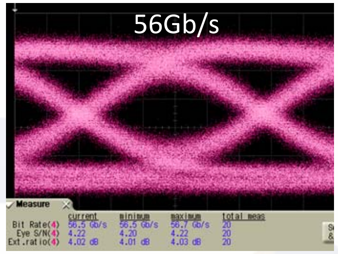
- Within-device channel spacing control (2.4nm) 3-σ < 0.6nm
- Within-wafer resonator free spectral range (14nm) 3-σ < 0.25nm
- Within-wafer channel wavelength control 3-σ < 8.0nm

Note: data is based on multiple wafers / multiple lots

ISIPP25G+ Performance: Actives

Ring Modulators

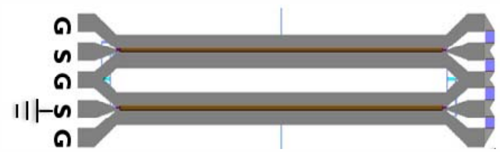


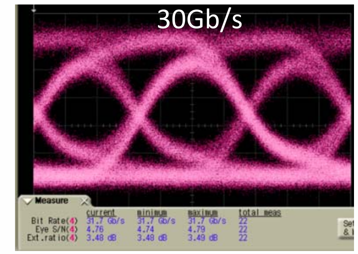


- 56Gb/s achieved with 2.5V_{p-p} (ER=4dB)
- Transmitter Penalty @1V_{p-p} <9dB
- Modulation efficiency 39pm/V

Note: this result has been achieved on 300mm wafer

MZI Modulators

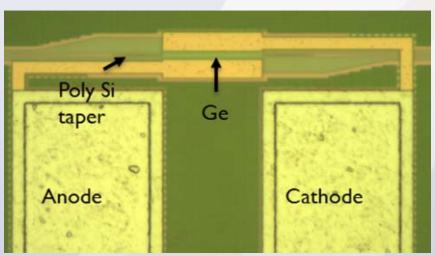


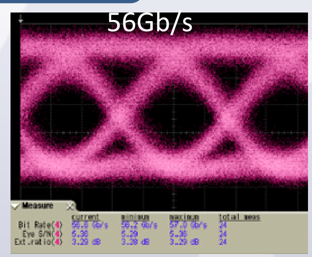


- 30Gb/s achieved with 2.0V_{p-p} (ER = 3.5dB)
- V_π-L_π = 1.0V.cm, Insertion loss = 6dB
- On-chip electrode term., single-ended drive

Note: this result has been achieved on 300mm wafer. Improved performance expected with push-pull configuration

Ge EA Modulators

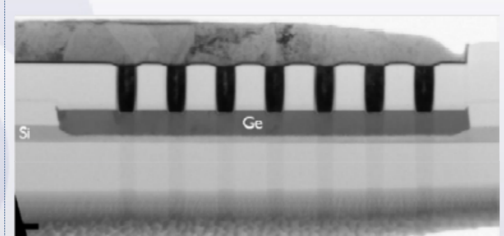


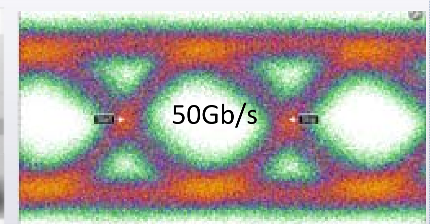


- 56Gb/s achieved with 2.0V_{p-p} (ER=3.3dB)
- Transmitter Penalty @2.0V_{p-p} <9dB
- Operation at 1610nm

Note: optimization for C-Band modulation on-going

Ge-on-Si Detectors



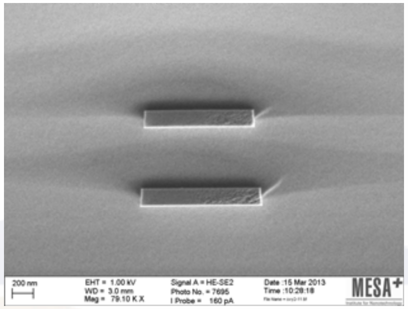


Typical Performance at -1V, Room T., 1550nm

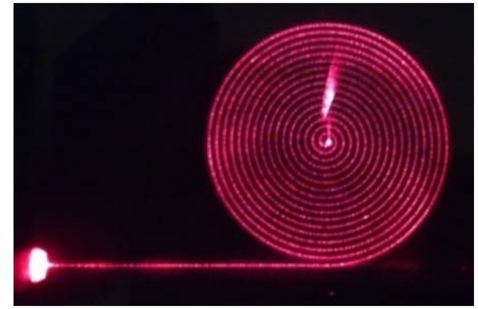
- Device Type I: 0.85A/W, <30nA, 51GHz
- Device Type II: 0.97A/W, <30nA, 23GHz

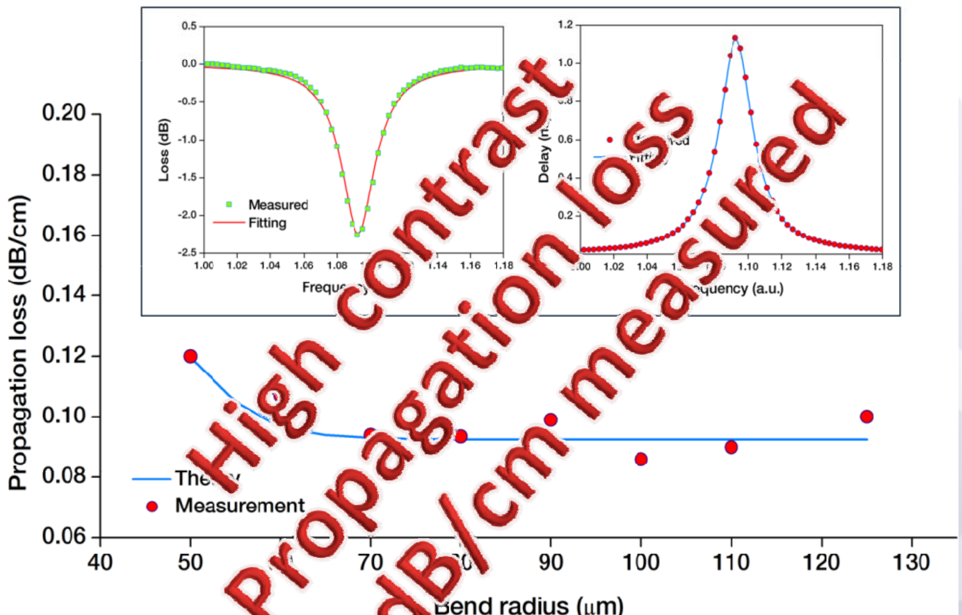
Note: the data is based on multiple wafers / multiple lots

Introducing TriPleX: Ultra Low Loss



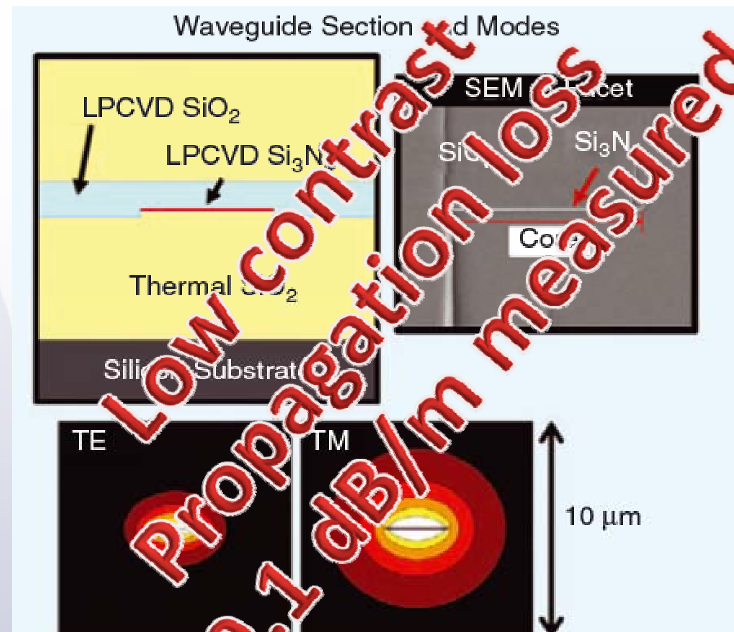
LPCVD
Si_3N_4 + SiO_2
platform





High contrast
Propagation loss
0.1 dB/cm measured

Zhuang, Leimeng and Marpaung, D.A.I. and Burla, M. and Beeker, W. and Leinse, A. and Roeloffzen, C.G.H. (2011) *Low-loss, high-index-contrast Si_3N_4/SiO_2 optical waveguides for optical delay lines in microwave photonics signal processing* Optics express, 19 (23). pp. 23162-23170

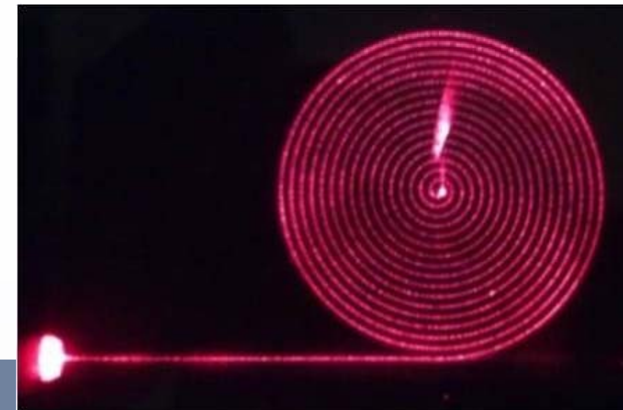


Low contrast
Propagation loss
<0.1 dB/m measured

"An Ultra-Low-Loss (<0.1 dB/m) Planar Silica Waveguide Platform," Bauters, Jared F; Heck, Martijn J R; John, Demis D; Barton, Jonathon S; Bruinink, Christiaan M; Leinse, Arne; Heideman, René G; Blumenthal, Daniel J; Bowers, John E, IEEE Photonics Newsletter, December 2011, p. 4-6, December 9, (2011)

TriPleX Offers MPW & Custom Runs

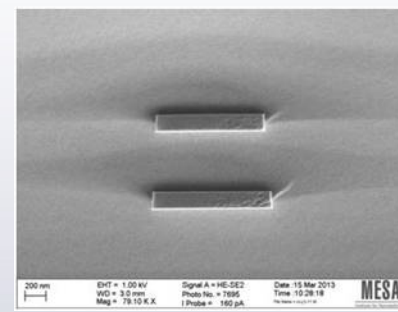
- Photonic ASIC prototypes in TriPleX MPW fab (typically a run every 4 months)



- Low-loss dielectric waveguides :
  - silicon nitride
  - silicon oxide

✓ High Quality Passives (AWG, MZ, ring, ..)
✓ Low-loss waveguides ≤ 0.5 dB/cm
✓ Bend radii 125 µm allow real VLSI
✓ Spotsize converters for low coupling loss
✓ Thermo Optic Phase modulators

Visible light to IR transparency (405 to 2350 nm)
Packaging services for prototypes available via XiO Photonics

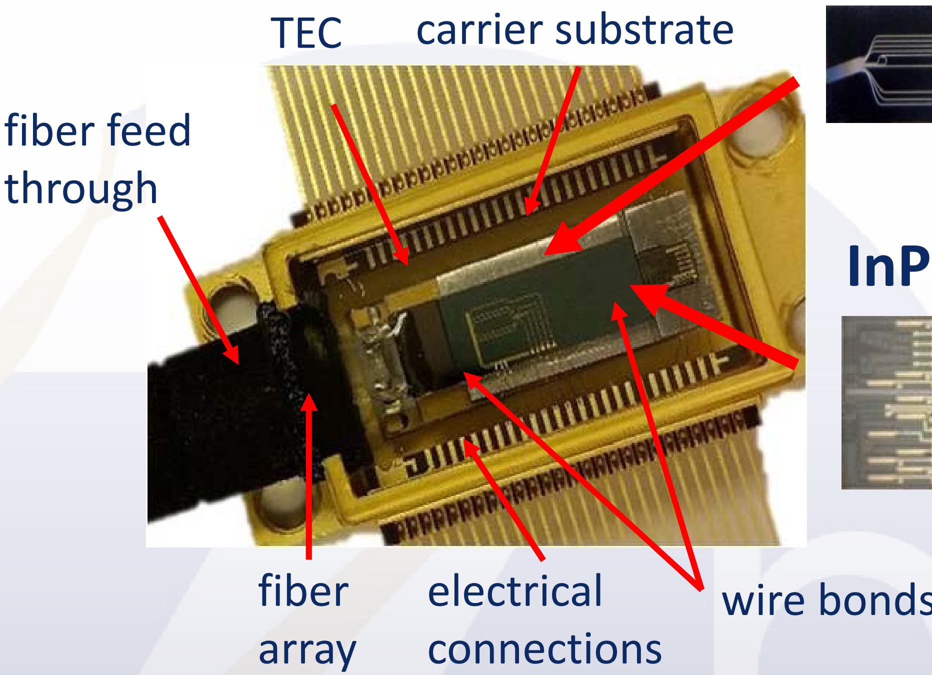


XiO photonics — Excellence in integrated optics

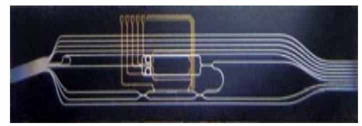
www.lionixbv.nl/triplexmpw

LioniX — OUR CHIPS ENABLE YOUR PRODUCTS

TriPleX Combines Well With InP

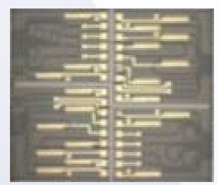


TriPleX chip



Low-loss waveguides & spot-size converters
Visible & NIR ranges

InP Chip



Active devices
Lasers, SOAs, fast modulators + PDs

- Combine the best of both worlds

Comparison of Costs for MPW PICs

Broker	Process	MPW die size mm²	Price EUR	MPW cost/mm²	Chips per MPW run	Material
JePPIX	SMART TxRx 10	2 x 4.6	4500	500	8	InP
JePPIX	HHI Rx 40	3 x 6	5500	300	8	InP
JePPIX	Oclaro TxRx 10	2 x 6	12000	1000	8	InP
TripleX	TriPleX	16 x 16	16000, 8500*	63	4	Si_3N_4/SiO_2
Europractice	Imec PSV	3 x 6	5000	278	>25	Si
Europractice	Imec ISIPP25G+	2.5 x 2.5	10000	1600	>10	Si
Europractice	CEA-LETI Si310-PH	1.7 x 3.7*	6610*	1050	15	Si
Europractice	IHP PIC	custom	Size scaled	2000	20	Si
VTT	VTT 3 µm SOI	5 x 10	8000	160	8	Si

- InP MPWs: 2”- 3” wafers, 50 – 200 chips per wafer
- Silicon Photonics MPWs: 6”-8” wafers, 300 – 5000 chips per wafer
- Perception is that Silicon Photonics is more cost effective at high volume (e.g. datacom)
  - Table shows that InP is cost effective relative to Silicon Photonics
  - Question is what the high volume is and at which cost metrics changes

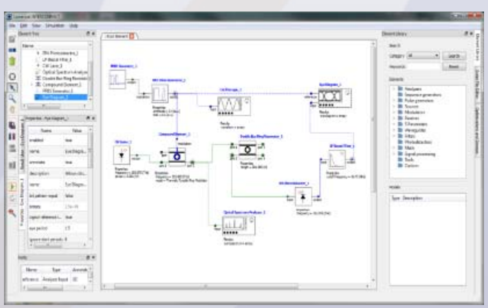
Design Software and PDKs

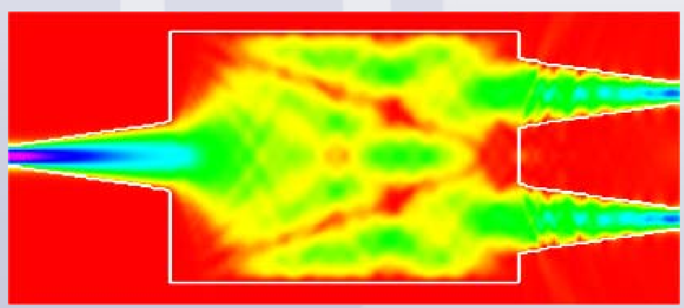
PIC Design Software

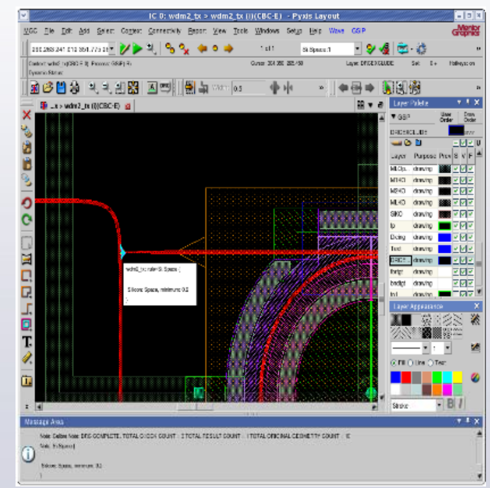
- Fortunately, these days really good S/W is available
  - It goes w/o saying that EDA tools were created for Electronic ICs
  - Likewise Photonic Design S/W has been created for PICs
- But there are in between situations:
  - What if your chip has optical as well as electrical components?
  - What if you plan to do the photonic simulations in PDA, but then use EDA for the mask layout?
  - Also, there are ongoing efforts between EDA and PDA providers to make their S/W interoperable and support the industry to scale from R&D to (volume) manufacturing
- Even though some functions can be done using both PDA as well as EDA, some care is needed…

EDA and PDA: Photonics ≠ CMOS

- Integrated Photonics has “RF-like” behavior, requiring:
  - Dedicated photonics simulation routines
  - Accurate and flexible definition of all angle shapes
  - Control of phase relations
  - Libraries with parametric photonics building blocks
  - Special features for verification (DRC, LVS)

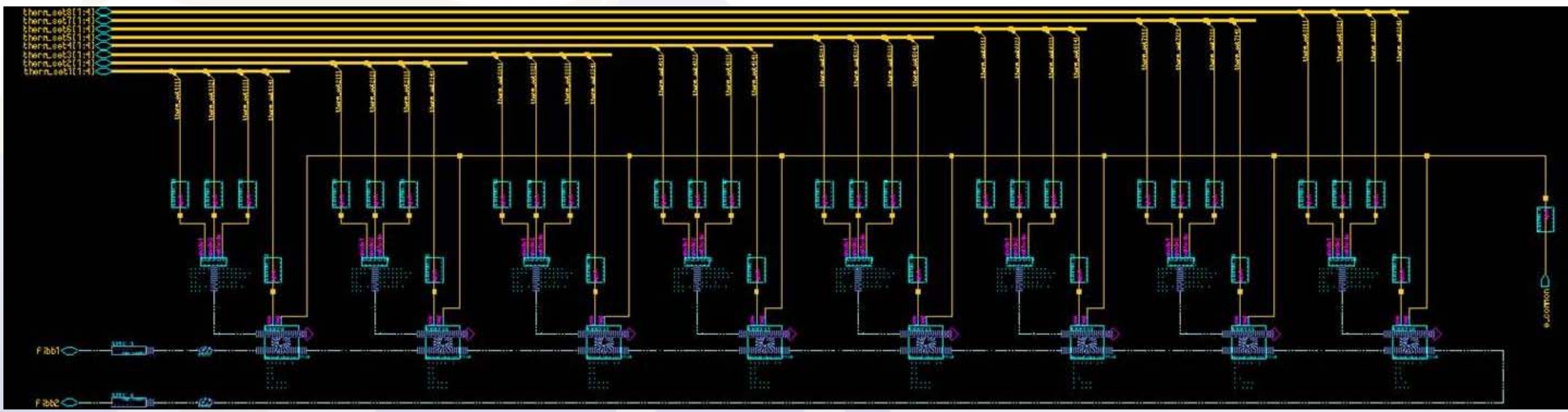


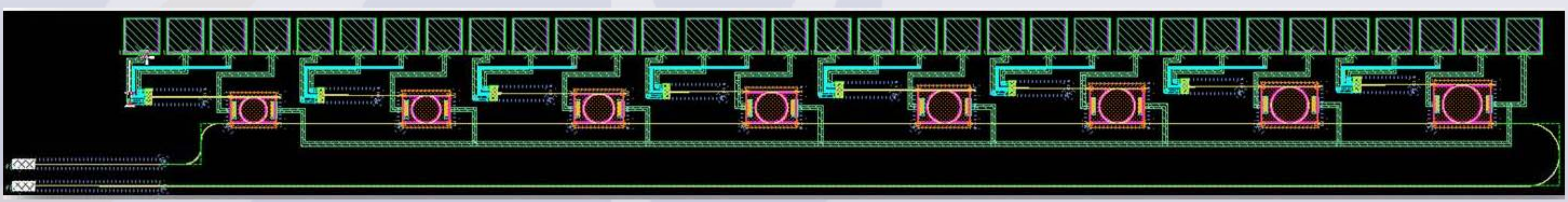




Tools support design at circuit level

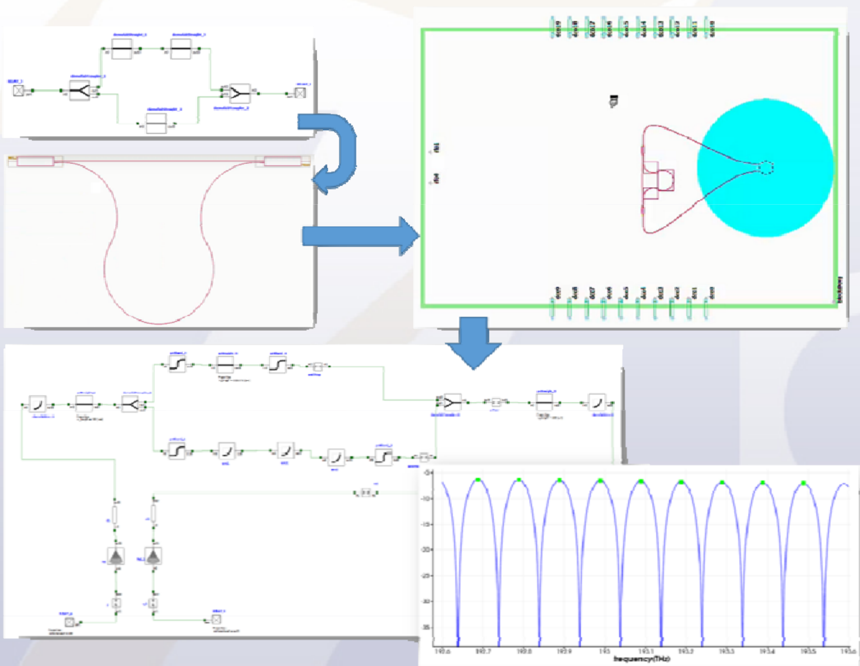
- Pick, place and connect validated components
- Photonic and electrical connections automatically detected
- Schematic connectivity drives layout directly

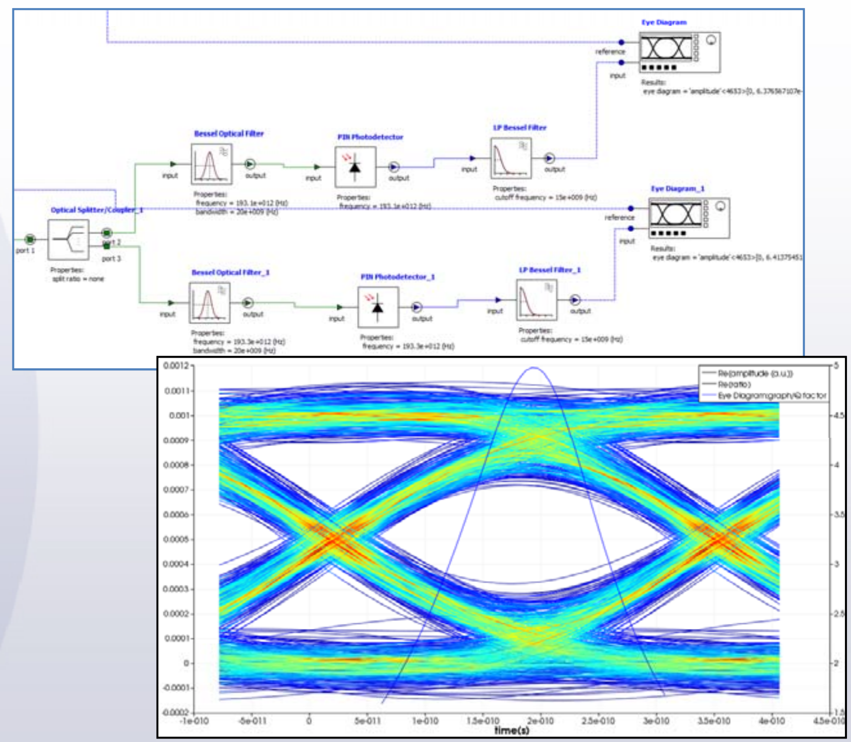




Tools support circuit simulations

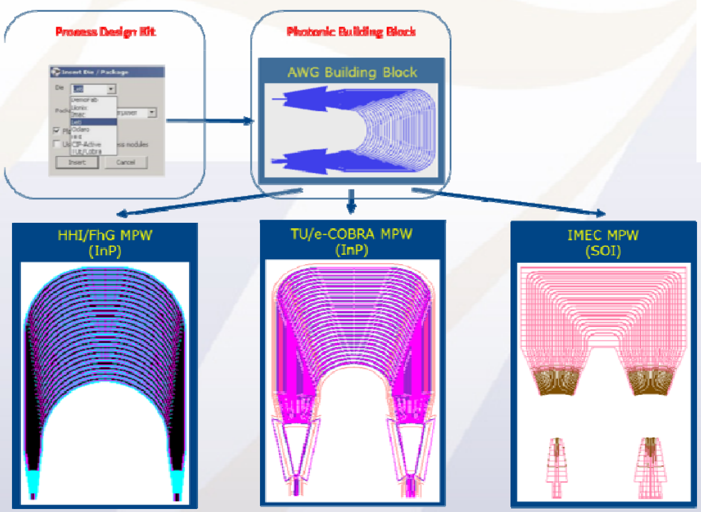
- Calibrated model libraries improve design accuracy
  - Design using compact model libraries of fundamental and complex devices, calibrated to foundry processes
  - Frequency & time domain simulation

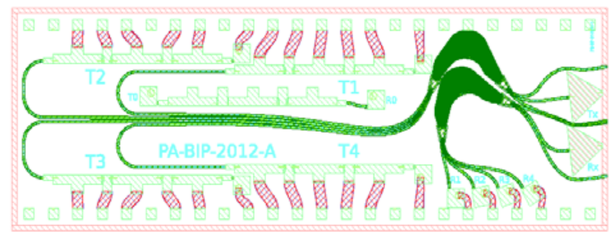




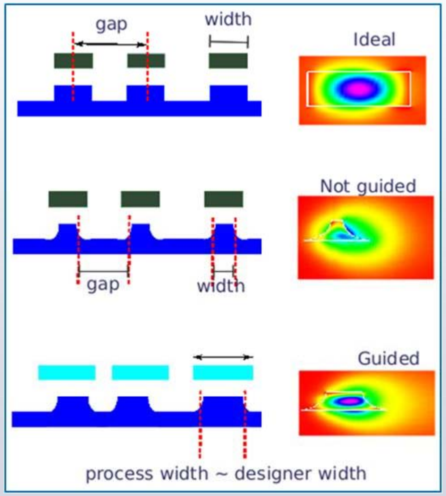
Tools support mask layout generation

- Design S/W can translate design intent into layout
- Design S/W can correct for process influences

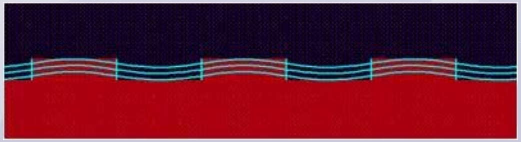


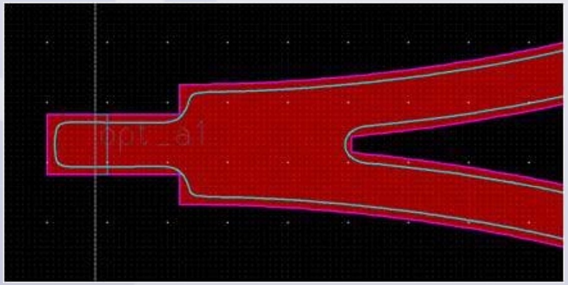


Use technology information to obtain design intent after fabrication



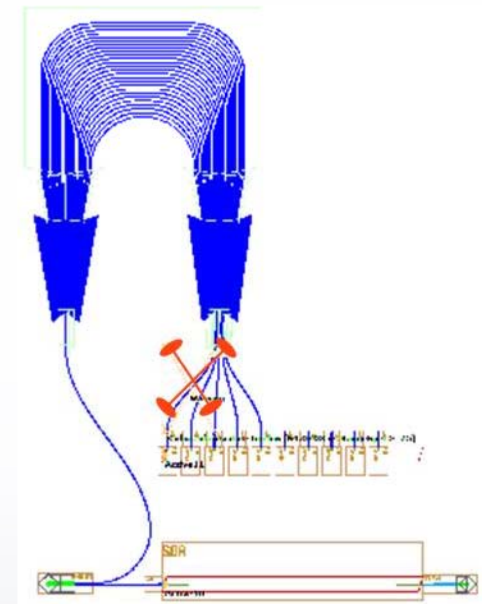
Simulating lithography influence on design intent

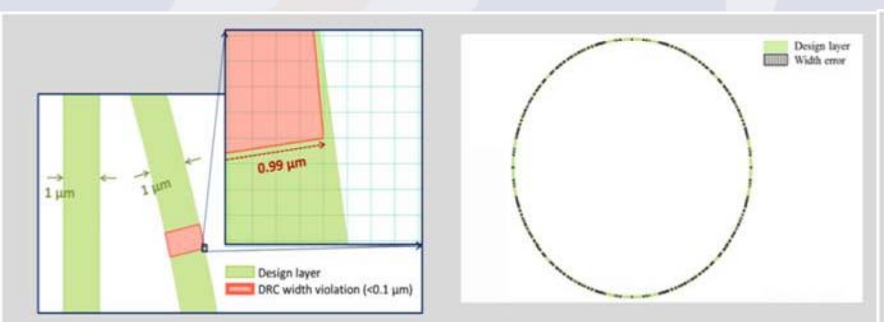


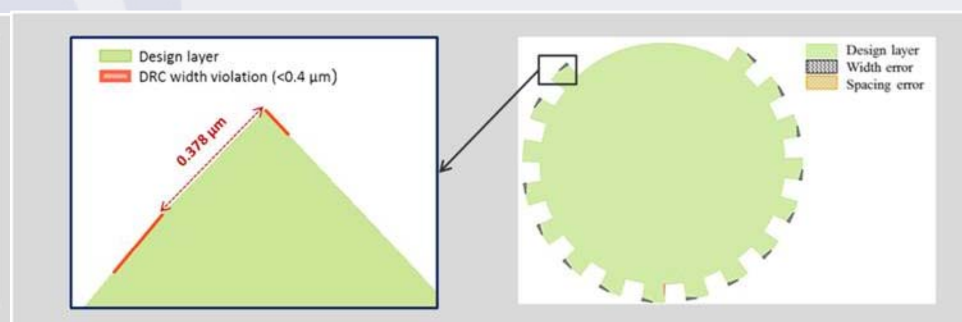


Tools support design verification

- Functional verification, Design Rule Checking (DRC) and Layout vs Schematic (LVS)
- Built-in photonics relevant design checks
  (like minimum bend radius)
- Design rules targeting CMOS processes will flag thousands of false errors in photonic structures, Photonic specific DRC rules can minimize false errors
- Integrated design flows enable LVS







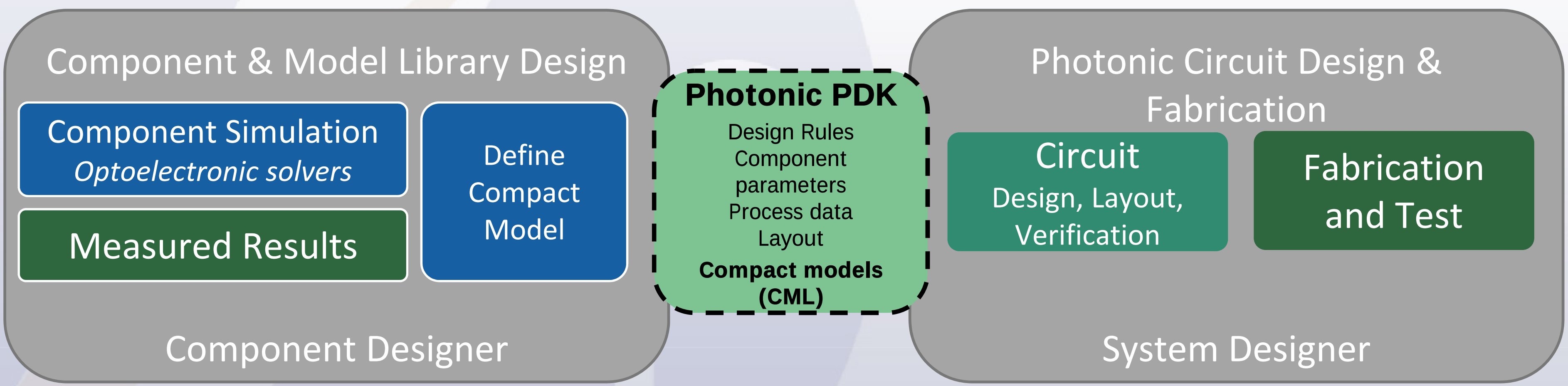
Why are PDKs so important?

- When working with a foundry (or your own fab), you do not want to reinvent the wheel nor make unnecessary mistakes
  - So all relevant knowledge should be available when designing a PIC
  - And the PDK should be automated (rather than in the form of docs)
  - Without a PDK, there are simply too many unneeded iterations
- What does a PDK include?
  - Design rules and mask layer information
  - Library of validated components
  - Layout information
  - Simulation models and settings
  - Die and package templates

PDKs enable efficient development

Faster design cycles and first-time-right designs

- Higher accuracy by using validated compact model libraries for circuit design
- Faster layout implementation by using predefined parametric components
- Higher yield in manufacturing by applying design rules



A wide variety of PDKs is available

- Foundries:
  - Silicon: IMEC, CEA-Leti, VTT, IHP and IME
  - InP: FhG/HHI, Oclaro and SMART Photonics
  - TriPleX (SiN): LioniX
- Packaging: Technobis ipps, Chiral Photonics, Gooch and Housego, Linkra, XiO Photonics and Tyndall
- PDKs are available to a varying degree of maturity
- PDKs are typically made available through MPW brokers

PDKs support integration of design flows

Schematic Capture
INTERCONNECT
Lumerical Solutions

Layout and Mask Generation
OptoDesigner
PhoeniX Software

PDKs
Design Rules,
Compact Models
Component Parameters
Process Data

Photonic Circuit Simulation
INTERCONNECT
Lumerical Solutions

Verification
LVS, DRC
PhoeniX Software

Compact Model Parameter Extraction

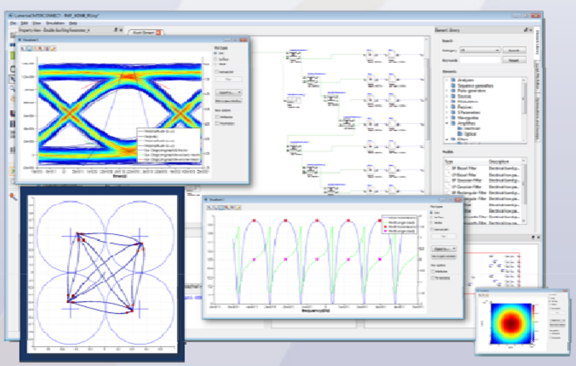
Optical Parameters Define Layout Structures

Photonic Component Design
Optoelectronic solvers, Experimental data

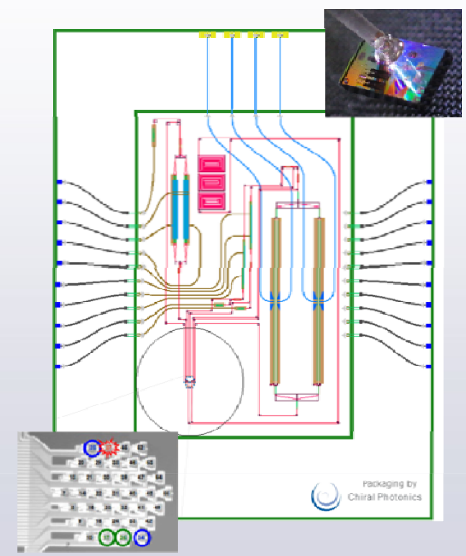
Lumerical Solutions

PhoeniX Software

lumerical

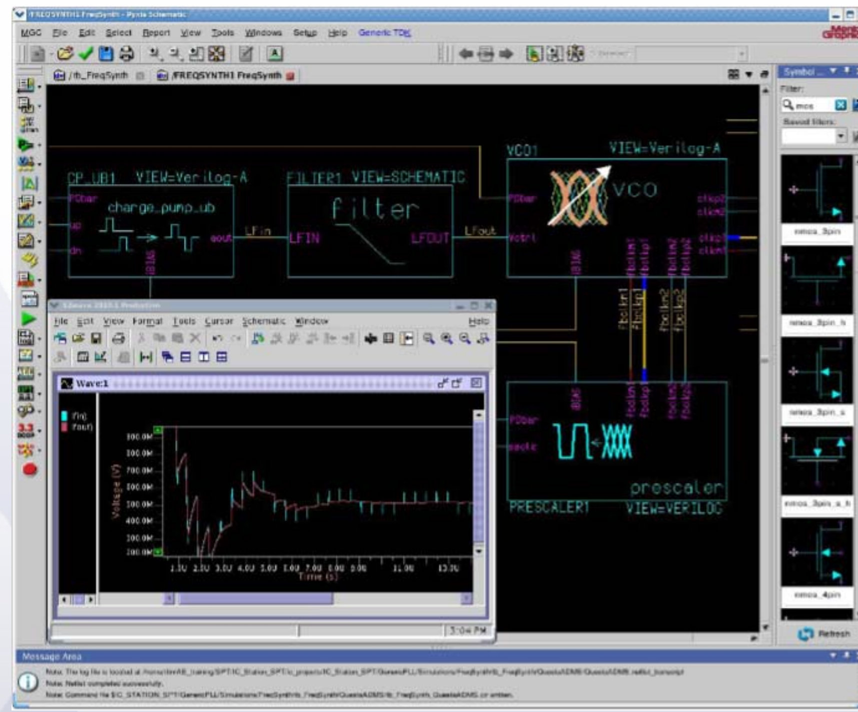


PhoeniX Software
Solutions for Micro and Nano Technologies

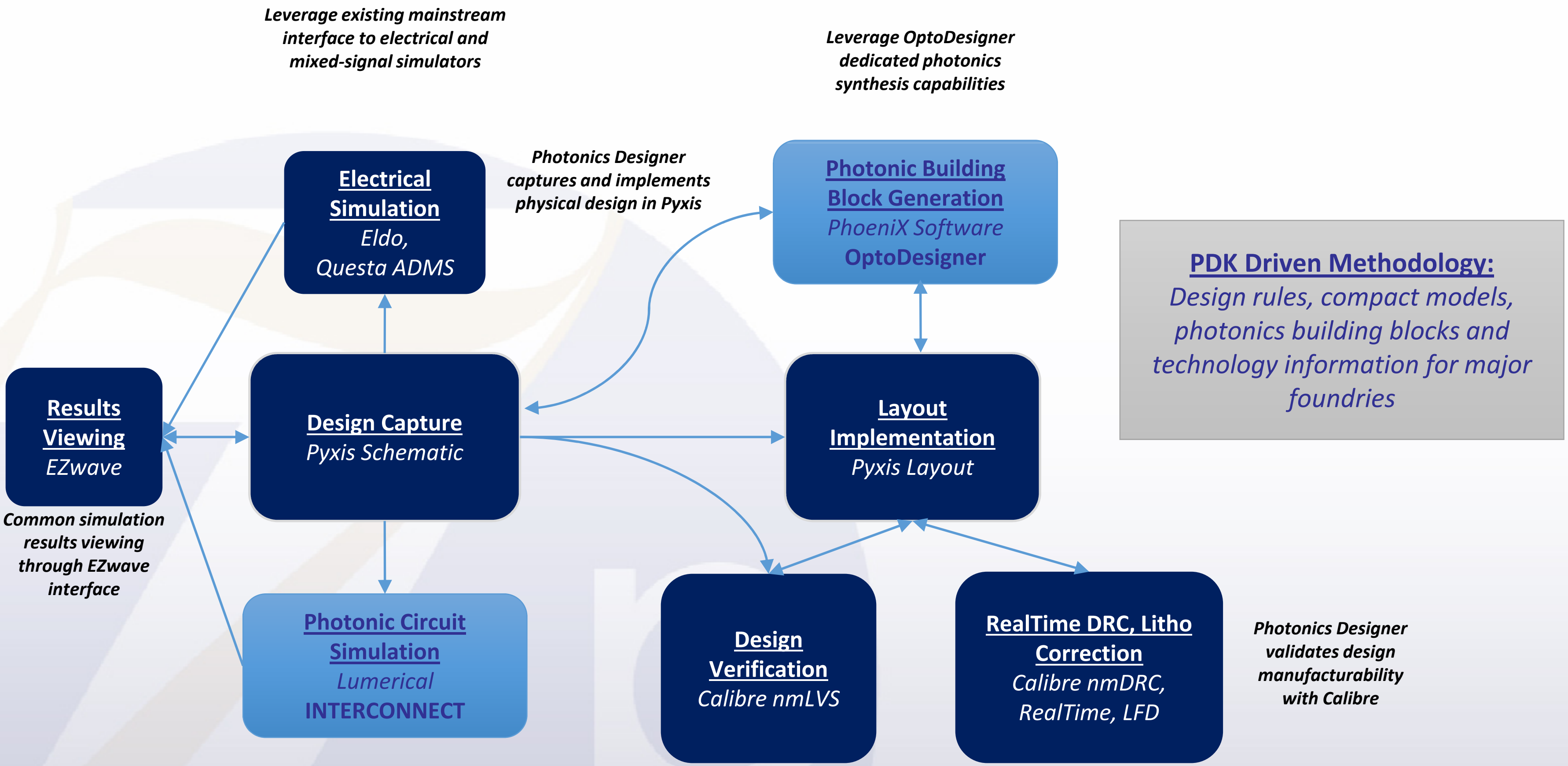


Scaling Silicon Photonics

- As in the electronic IC ecosystem, faster and more complex photonic ICs will require multi-user collaboration
- Innovators will need to build teams with dedicated expertise in multiple areas of PIC design – from system concept to physical layout
- Mentor Graphics provides the tools to do this:
  - Pyxis enables multi-user collaboration in common environment
  - Calibre provides sign-off assurance through physical verification

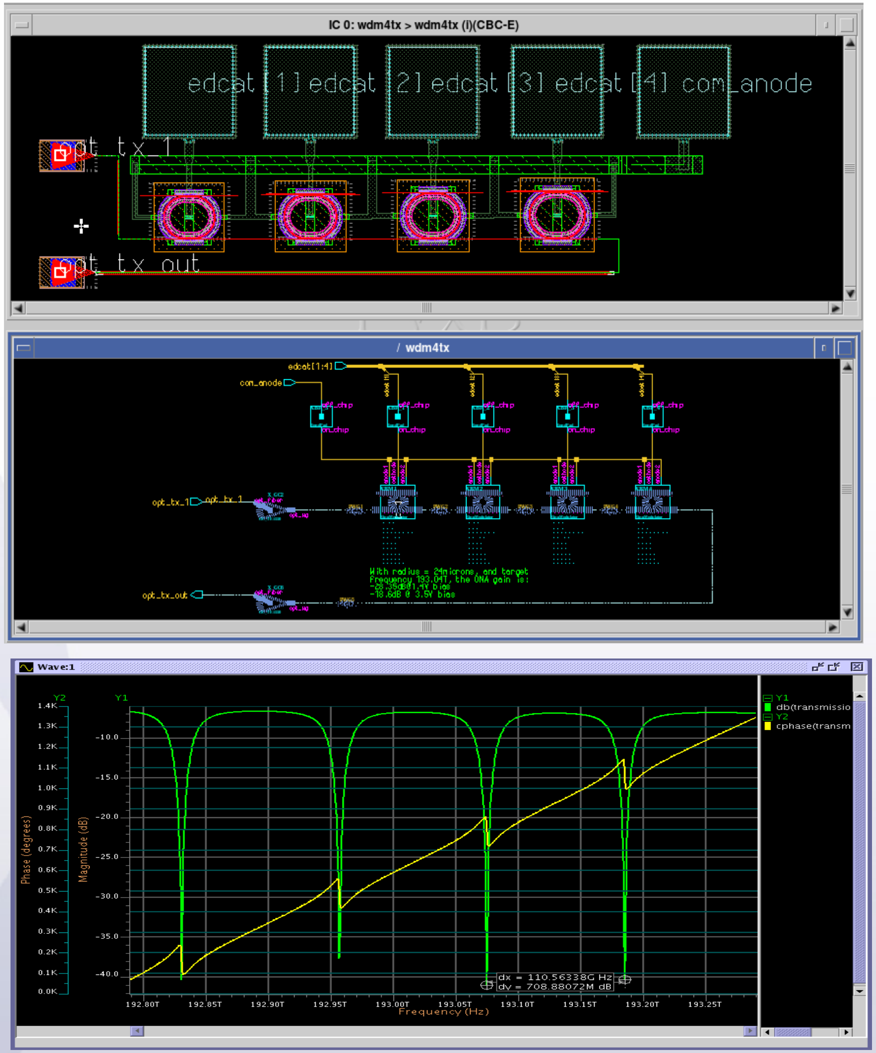


EDA Driven Design Flow



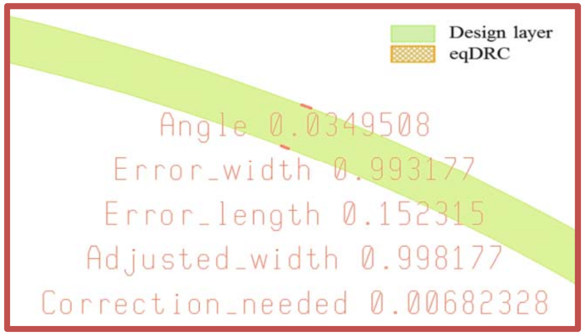
Why Pyxis?

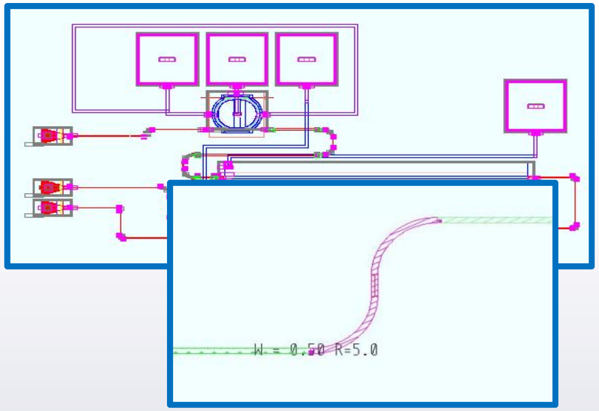
- Provides a collaborative multi-user environment
- Simulate schematics using Lumerical INTERCONNECT, Eldo with Verilog-A, or Questa ADMS
- Flexible infrastructure allows quick integration to any tool accessible within Linux
- Complete PDK driven design flow leveraging Calibre, Lumerical and PhoeniX Software

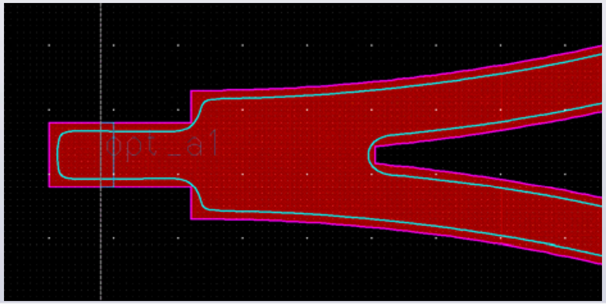


Why Calibre?

- Market and industry standard
- Fast and accurate DRC:
  - EqDRC handles complex curves
  - RealTime results in Pyxis
- Photonic LVS:
  - Shorts & opens detection
  - Device validation
  - Waveguide interconnect parameter extraction
- Lithographic Modeling:
  - Reduces manufacture iterations
  - Drive accurate photonic simulation







Why Lumerical?

Three Distinct Design Activities for PIC Development

1. Component-level design and optimization
   - Design and optimize a component for desired performance

User / Designer

2. Compact model library generation for PDKs
   - Build compact model for component
   - Calibrate against experimental results
   - Inform with simulation results

User / Designer
Access Partners
Fabrication Packaging

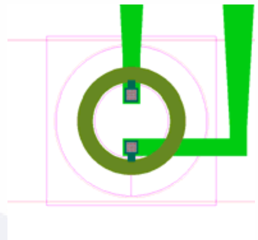
3. Photonic Integrated Circuit design and optimization
   - Build complex circuits based on known components with validated compact models

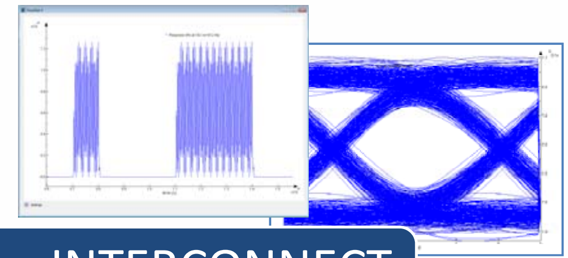
User / Designer
Access Partners
Fabrication Packaging

Why Lumerical?

PDKs
Design Rules,
Compact Models
Component
Parameters
Process Data

Layout Information
Process Information
Design Rules





INTERCONNECT
Photonic Integrated Circuit
Simulator

Compact Model Library for
Circuit Design &
Optimization

Photonic Component Design
Optoelectronic Solvers,
Experimental Data

Compact Model
Parameter Extraction

FDTD Solutions
Nanophotonic Solver
(2D/3D)

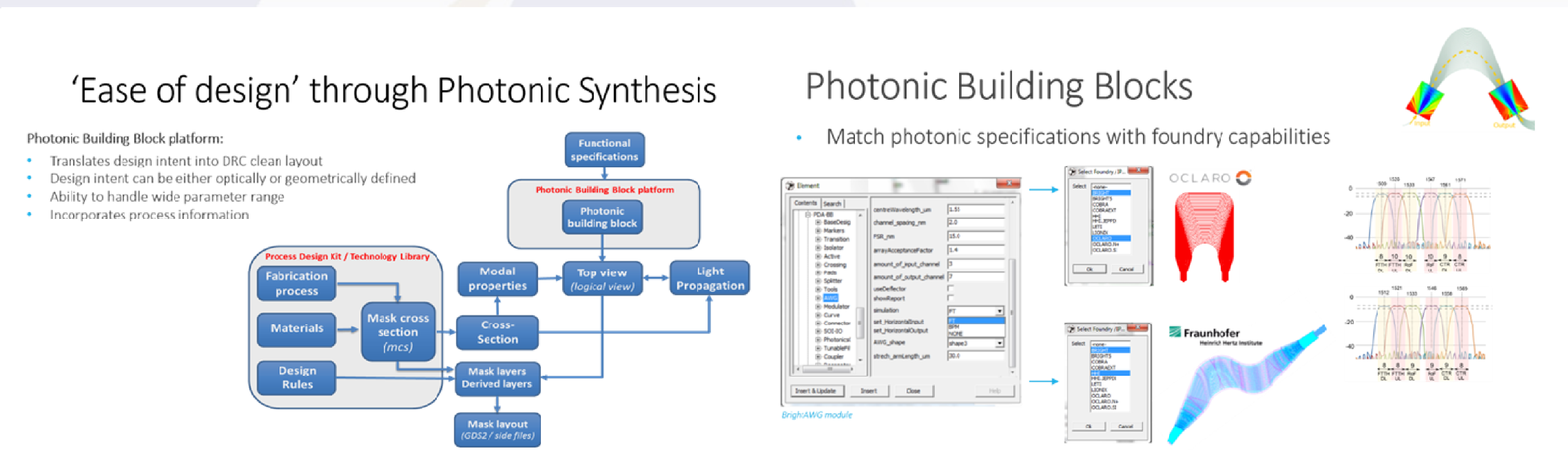
MODE Solutions
Waveguide Design
Environment

DEVICE
Charge Transport
Solver (2D/3D)

- Parameter Extraction for Compact Models
- Component Design & Optimization

Why PhoeniX Software?

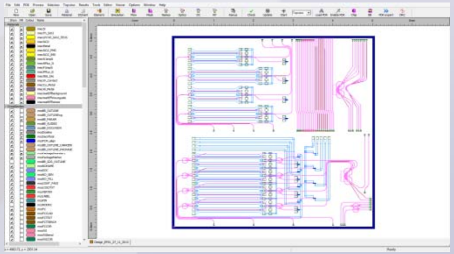
- Design for Manufacturability
  - Automatic translation of design intent into manufacturable layout
  - Simulations and layout combined in one environment
  - Include process variations into the design flow

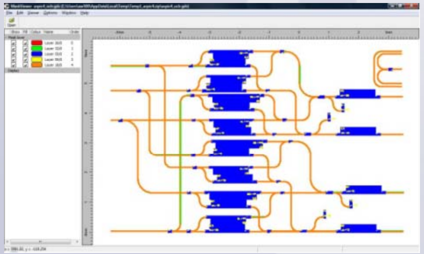


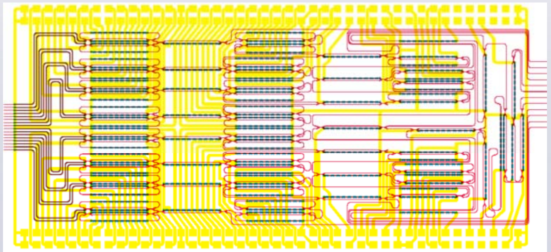
Why OptoDesigner?

- Native all-angle and all-shape design
- Complete parametrized library for photonics
- Includes photonics verification and design rule checking
- Interfaces with world-class 3rd party circuit simulators
- Easy to use GUI including powerful scripting
- PDKs available for 8 photonics foundry services

More than 300 designs created and fabricated in MPW's in the last 3 years!







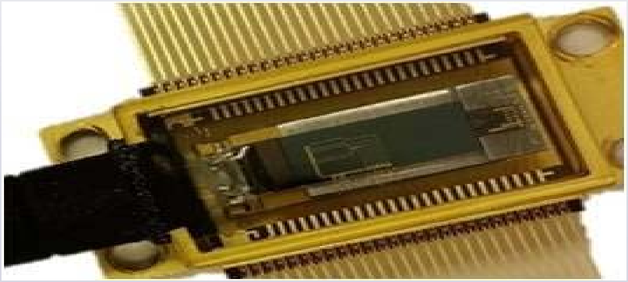
Packaging

Coupling, Packaging & Testing

Critical to discuss the device I/O and packaging at the earliest stages of design - assures efficient testing and design iterations

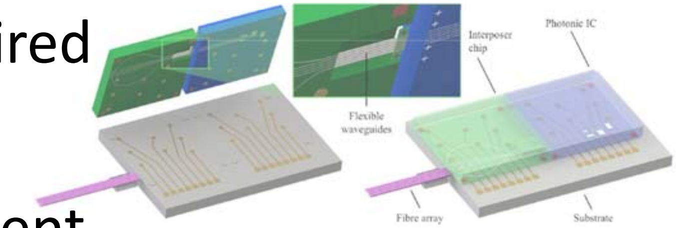
- Edge vs. surface optical coupling
- Active alignment design / equipment needs
- Testing / design verification needs
- Probing, optical and electrical (DC/RF), at wafer and die level
- Application-specific packaging needs, e.g.
  - Rudimentary, development package for interim testing & refinement of design
  - Thermoelectric cooler (TEC) and temperature sensing
  - Cryogenic testing
  - Hermetic package
  - Butterfly package or other specific package requirements
  - Pluggable vs. pigtailed package

Coupling Technique	Broadband	Polarization Maintaining	Alignment accuracy (μm)	Coupling Loss (dB)	Edge preparation	Min channel spacing (μm)	Channel count per port
Edge	Yes	Yes	0.2	2	Yes	12	10s
Surface	No	No	1	3-4	No	37	100s

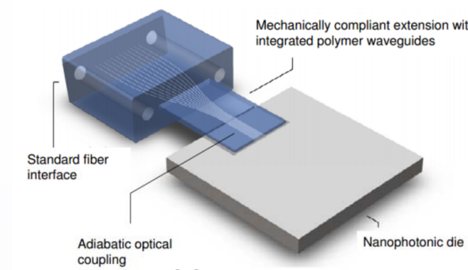


Packaging Resources

- Complex heterogeneous integration is required for PICs, which is not simple



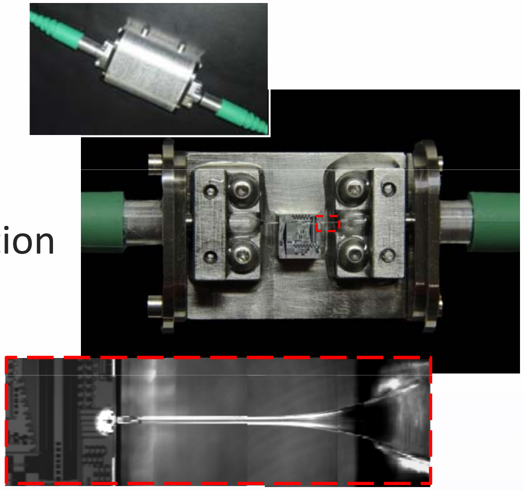
- Longer term projects pursue passive alignment solutions, e.g.
  - FP7 initiative PHASTFlex (http://www.phastflex.eu)
  - IBM's Compliant Interface



- Current state-of-the-art requires active alignment but offers scalable processes with available design help:
  - Some MPW foundries offer prototype packaging
    - JePPIX => Linkra, G&H and Technobis
    - Europractice => Tyndall (foundry has specific design rules for Tyndall packaging)
    - LioniX => XiO Photonics
  - Chiral Photonics (New Jersey, USA) offers dedicated optoelectronic packaging and testing services in addition to consulting and enabling components

Chiral Photonics

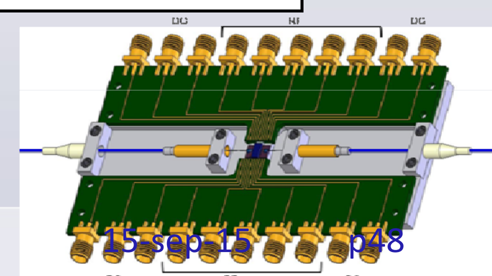
Chiral Photonics



- Design consultation
  - Complimentary coupling and packaging guidelines: DesignGuide@chiralphotonics.com
  - Discuss critical design elements, e.g.:
    - Channel and port placement
    - Optical passthrough (e.g. extra channel, port) vs. on-chip detection for alignment
    - Fiducial markings
    - Die edge preparation
    - Initial design verification and testing requirements, e.g.:
    - Wafer and die probing
- Development packaging & fundamental testing
  - Designed to facilitate electrical/optical probing
  - Standard packages supported by design software, e.g.:

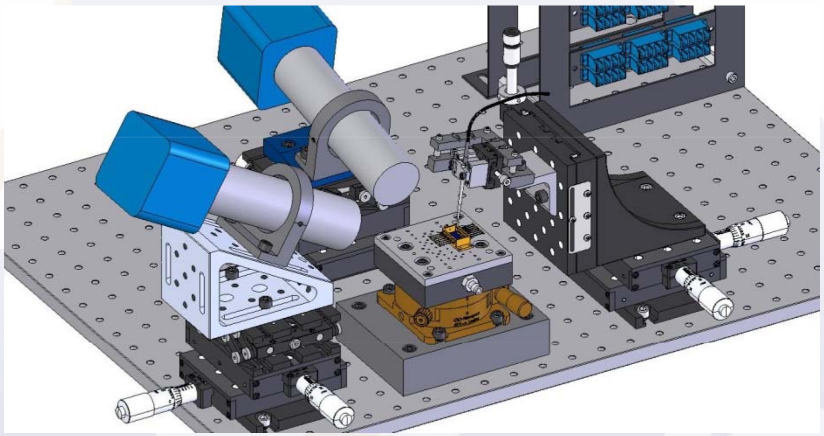
	APPROX. PRICE (USD) 1st die / Subsequent die (small quantity)
Optical Only – 2 single-channel ports	4,000 / 3,200
Optoelectronic – 2 single-channel optical ports, 25 Gb/s (10 RF / 10 DC)	8,000 / 5,000
Optoelectronic – 2 single-channel optical ports, 50 Gb/s (10 RF / 10 DC)	9,000 / 6,000

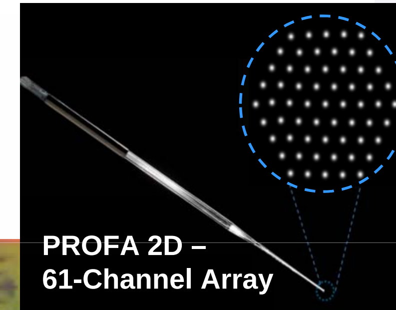
  - Characterization of packaged devices:
    - Broadband PM Spectra: TE vs. TM coupling, 1200-1700 nm
    - Waveguide edge mode field diameter measurements

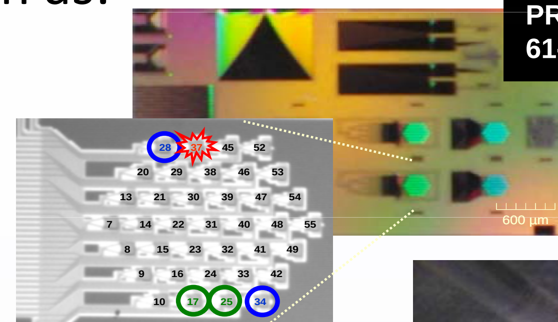


Chiral Photonics

- Fiber Optic Couplers, ultrahigh density
  - Surface and edge coupling PROFA1D and 2D
- Probing and packaging equipment, such as:
  - Surface optical probing equipment

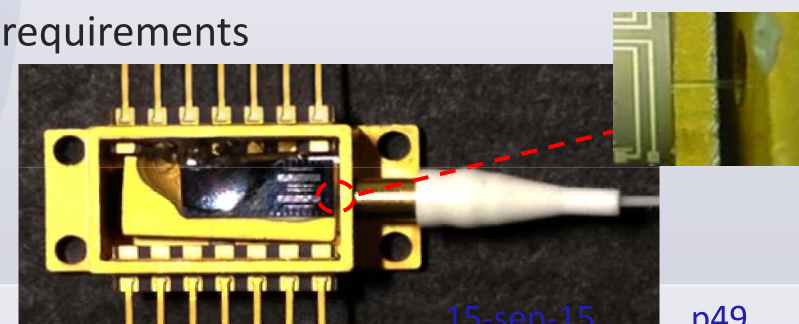






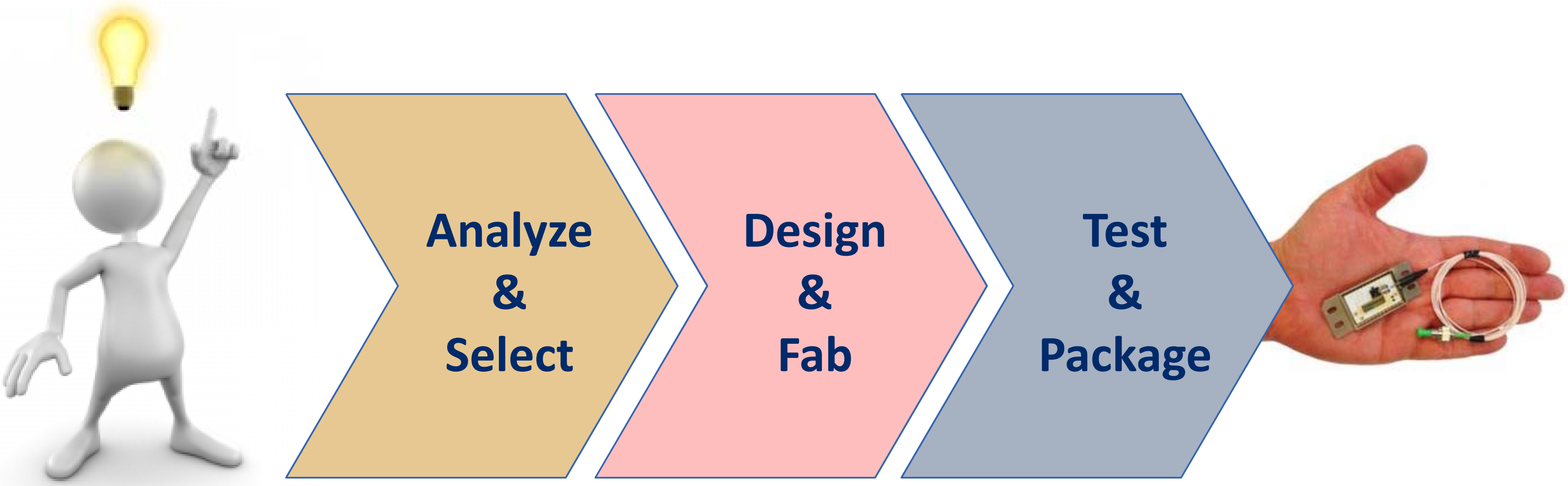
Same equipment used to couple 37 channels simultaneously, with 3 dB coupling loss, to imec PIC:
V. I. Kopp, et.al. JLT, 33, 3, 653 (2015).

- Application-specific and production packaging needs
  - Meet specific, full optoelectronic application needs, such as:
    - Butterfly package or other specific package requirements
    - Cryogenic testing
    - Hermetic package
    - Pluggable package



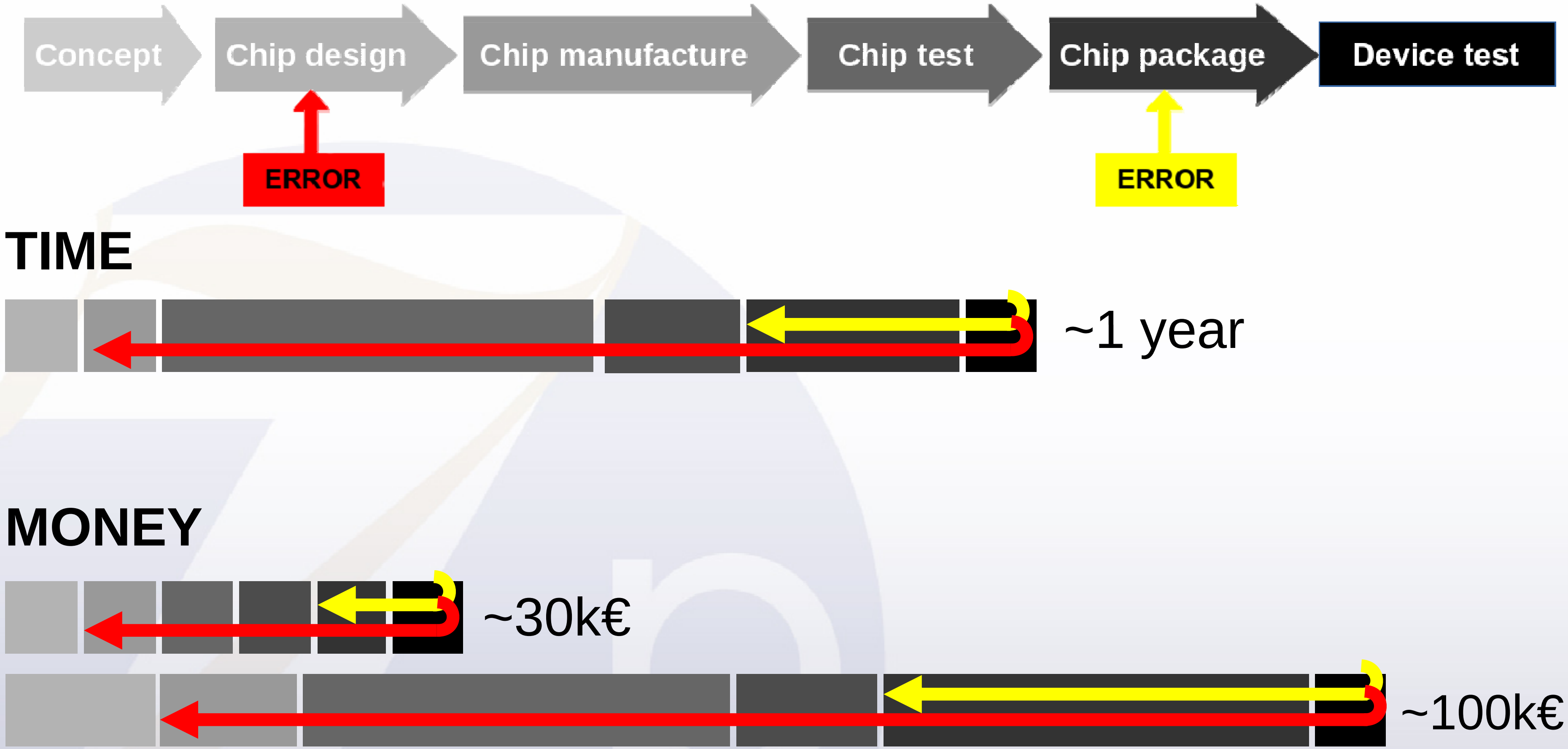
Turn-Key PIC Design Houses

Design Houses Support PIC Creation



- Turn-key PIC design houses can be ideal:
  - if you need specific design support
  - or if you do not have the design capabilities yourself
- In addition, they can provide a complete service
  - This includes testing, packaging, and system level evaluation

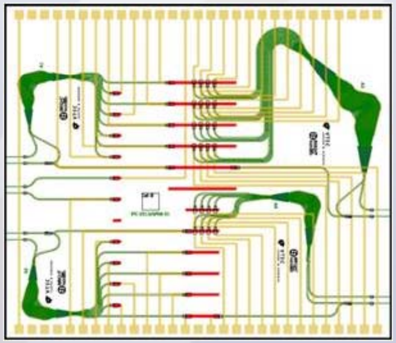
Design House Also Reduces Risks

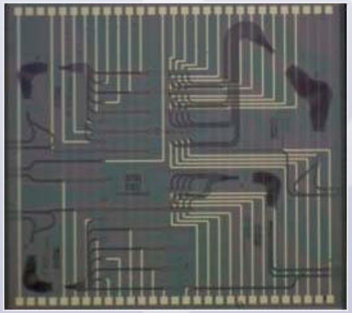


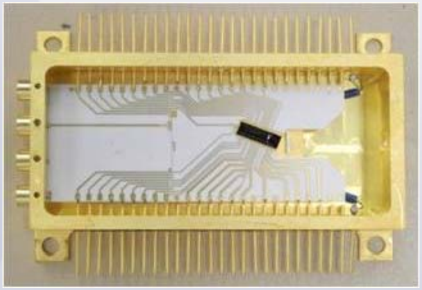
- Critical to minimize risk and ensure return on investment

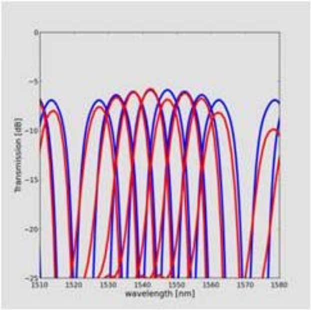
Design House Offer Several Benefits

- Get up to speed in no time: faster development
- Profit from experience: improve and validate designs
- Ensure optimal interfacing along the integration chain
- Total flexibility: from consultancy to turn-key solutions





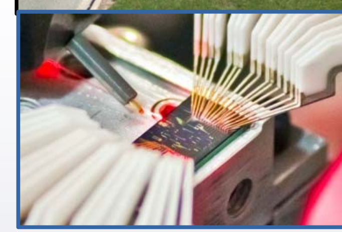




VLC Photonics' Design Services

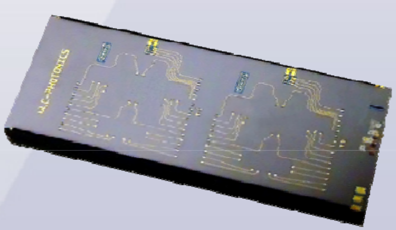
VLC Snapshot

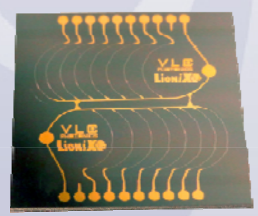
- Optical chip design and characterization in all photonic technologies
- Offices in Valencia, Spain, with representation in the Netherlands & USA
- 6 members of extensive academic and industrial experience, 12+ years in the field of integrated optics and photonics
- Telecom/datacom, quantum, sensing & microwave photonic expertise

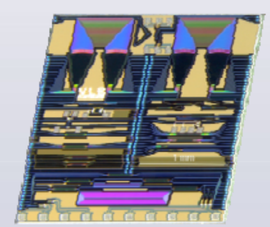


VLC's way of working

- Very fast reaction to work on all main platforms
- Confidentiality guarantees and complete IP transfer
- Optimized design libraries: AWGs, Echelles, MZIs, MMIs, etc.
- Extensive network of foundry and packaging partners







Why Bright Photonics?

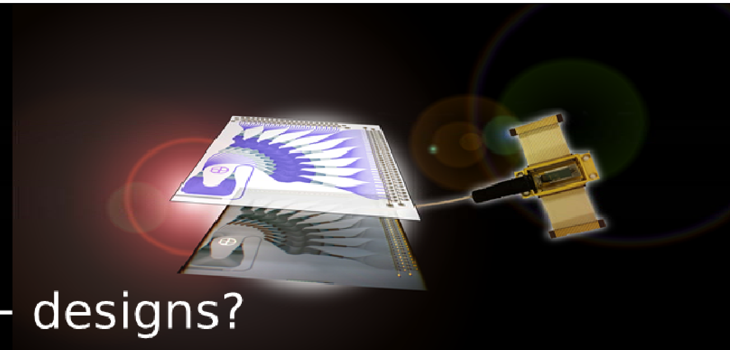
BRIGHT Integrated PHOTONICS

... just ask a design house ...

✓ Do your PICs make it into products?

✓ Are your design modules available to us?

✓ Did you do 20+ foundries, 25+ MPWs, 300+ designs?



Quick overview

Typical costumers:
- OEM, SME (products)
- Enterprises (R&D)
- Research groups

Partners and consortiums
- Partner network for PIC fab & pack.
- PHOXTROT (FP7)
- L3MATRIX (H2020)

Flexible cooperation formats with you
- 100% independent
- Quality saves most time
- We'll tell you if it isn't possible

What we offer

Products
- Co-development
- Prototyping
- Design for volume

Design
- Mask design &Training
- PDK implementation
- Design modules

Technologies
- SOI, SiN, Si
- InP
- Polymer, Hybrid

PIC Training

7pennies DEDICATED CONSULTING

Why Training Is Critical For PICs

- The way to go for PIC development is increasingly by using outside service providers
- You may need several providers and these all need to be working closely together (in the form of an ecosystem)
- This can all be hard to figure out, but the best way to find out is to actively engage in-depth during training
- This is where you become familiar with all the players and how they jointly produce seamless support
- In addition, the design and layout software is ideally tried in a guided training environment

Unique Training Event Held in North-America

- Date: Oct 19-23, 2015
- Location:
  Dept of EE,
  Columbia University
  New York City
- Material independent:
  covers Silicon, InP, & TriPleX
- Covers full range of system level, component tutorial, design & layout S/W, close to all MPW foundries, packaging, turn-key PIC design houses, business topics
- www.7pennies.com/news-events/pic-training-nyc-2015/

Training Supported by Broad Group

- Foundries
  - InP
  - Silicon Photonics
  - TriPleX

AIM Photonics

- Design software
- Packaging
- Design houses
- Organization: www.7pennies.com

It’s Time for Questions

You can submit a question using the question tool on your screen.

LIGHTWAVE

Thank you for attending.

More questions? Contact:

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