Photonics Design Automation and MPW Runs for Affordable Chip Production

design tools, design kits and collaboration

PIC TRAINING NYC 2015

COLUMBIA UNIVERSITY, NEW YORK, USA, OCTOBER 19-23 2015

TWAN KORTHORST

Who we are

Lumerical Solutions

- HQ in Vancouver, Canada, since 2003
- Design software for photonic technologies
- Circuit and physical simulation tools

Mentor Graphics

- HQ in Wilsonville (Or.), USA, since 1981
- Solutions for full flow custom design methodologies
- Leader in physical verification solutions

PhoeniX Software

- HQ in Enschede, the Netherlands, since 2003
- Chip design for micro and nano technologies
- Physical simulation and layout generation

Why integrated photonics?

Electronics market is mature

- Total electronic components markets is > 500B$, with IC's ~250B$
- Electronics Design Automation (EDA) market just under 10B$

Mature (silicon) electronics industry comes with

- Fabless business model dominant
- Good array of foundries (TSMC, GF, Jazz, IBM, etc.)
- Well developed EDA industry (Synopsys, Cadence, Mentor Graphics)

Existing technologies are reaching bandwidth limitations

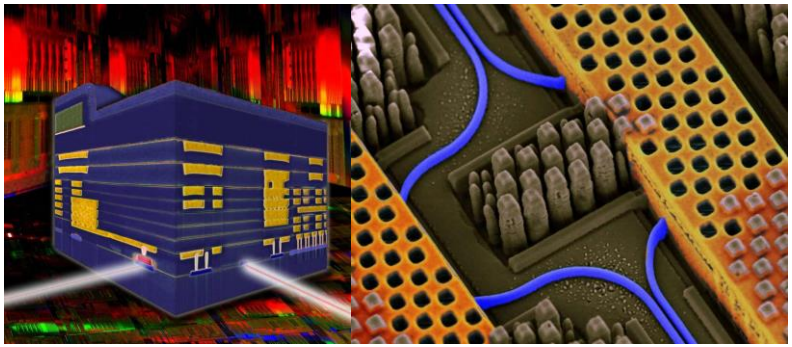
- Power consumption (heat) dominated by data transfer rather than computing
- Density

‘Photons will merge with electrons’

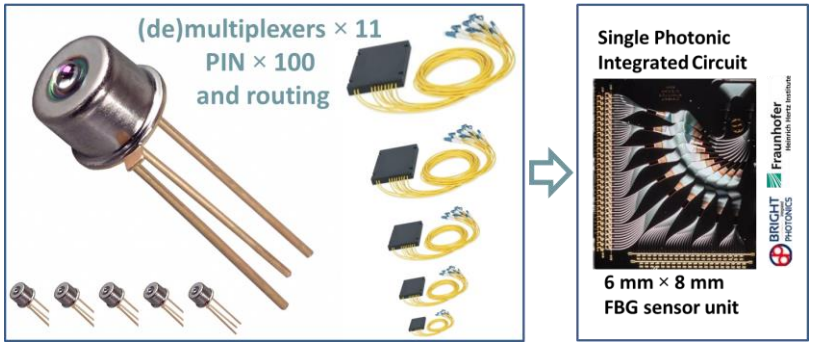
- Market need drives transition to integrated photonics solutions
  - Datacenters and High Performance Computing
  - 40G/100G/400G, FTTH
  - Microwave photonics (5G, nextgen wifi, LiDAR, …)
  - (Bio-)sensing
- Photonic Integrated Circuit market today relatively small (220M$)
  - Market size x4 by 2019, still only 0,4% of global IC market size
  - Today mainly InP based, performance driven
- Integrated photonics enables the transition by leveraging IC manufacturing technologies
  - Cost effective manufacturing (in volume)
  - Functions integration
  - High density
- Photonics technology is considered to be strategically important
  - Multiple Billion$ value in ‘transactions & investments’ recently
  - Photonics will become a significant part of the electronic IC market

There are many similarities between electronics and photonics

- Fabrication: thin film technologies, lithography
- Design flow: verified mask layout design as final step
- Photonics is where electronics was in the 80's
  - Transition from PCB to (silicon) IC
  - Large number of (small) fabs providing manufacturing capacity
  - Many software suppliers, each covering parts of the design flow
  - Emerging standardization in processes and tools



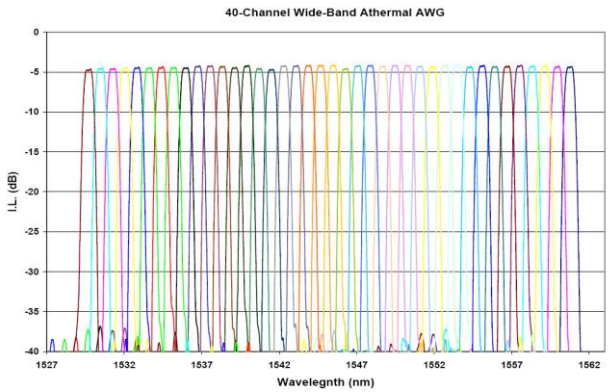
Source: IBM



With some key differences

Photonics industry today is dynamic and fragmented

- Wide variety of materials and technologies
  - Si / SOI, InP / III-V, PLC, TriPleX / SiN, LiNbO3, Polymers, …
  - Hybrids, 3D stacking, SiP
- Scalability roadmap is unknown
  - Typical line-widths: 0.15 – 4 micrometer
  - Number of components: 10's – 1000's per chip (relates to 10k – 1M primitives)
- RF-like or analog behavior (Telecom C-band is 1530 – 1565 nm ~ 193 THz)
  - Design closely related with fabrication
  - Process and temperature dependencies



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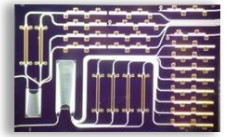
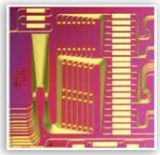
If you need a PIC, where do you go?

- You need an application specific PIC

Fiber to the Home
Wireless



Medical
Bio-imaging



Datacom
Switching

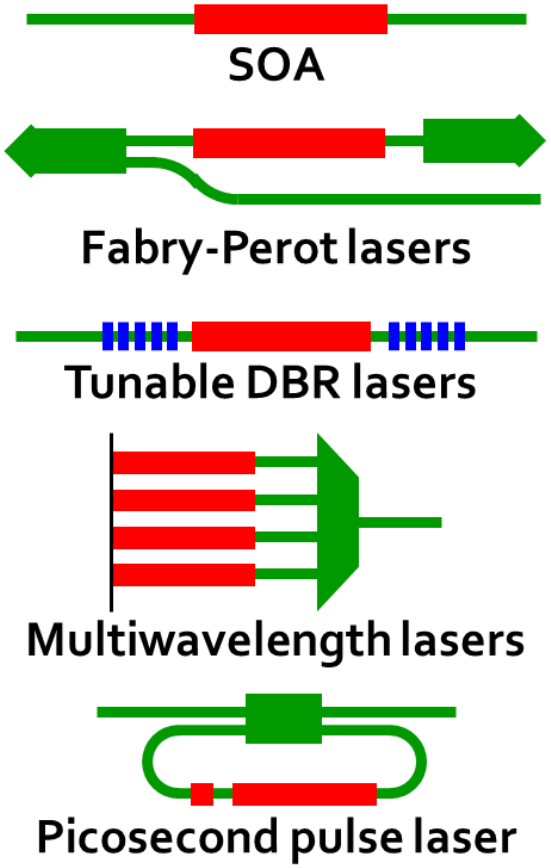
Sensor
Readouts

Please note that electronic ICs have paved the road for 50 years

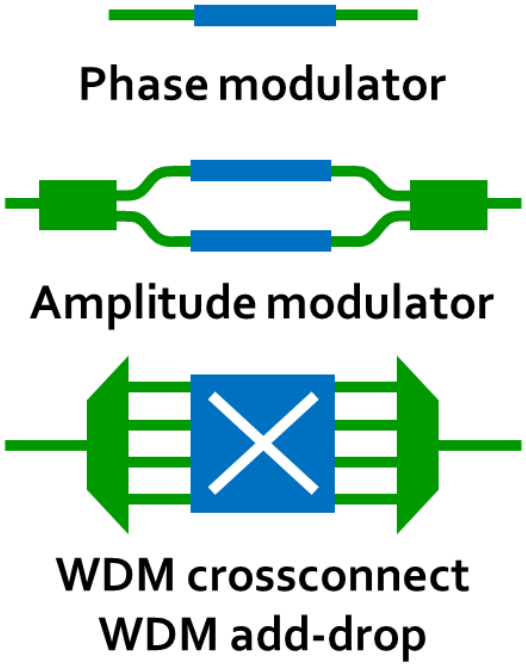
- You need to decide on material and foundry
  - Options: InP, Silicon, or TriPleX (excluding PLC and LiNbO3)
- Also need to decide on MPW vs. a custom run
  - MPW reduces costs, but custom runs might be needed in the end (for volume and/or for unique performance)

Decide on material

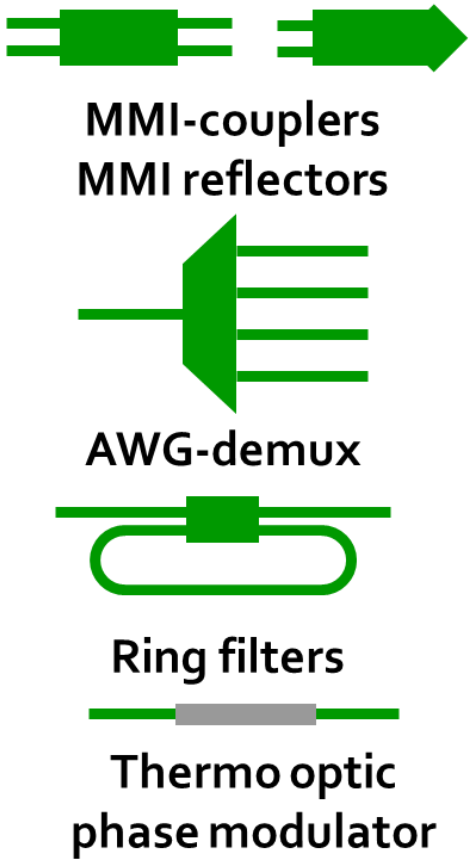
Active materials (lasers…) only possible in InP



Switches & modulators possible in InP & Silicon



Passives possible in InP, Silicon, and TriPlex



Decide on foundry

Multi Project Wafer runs versus Custom runs

- MPW users all share the same generic fabrication process
  - Cost sharing: multiple designs at same mask/wafer
  - Imposes limits, but comes with a library of building blocks
  - “Lego” building blocks allow for virtually all PICs
  - >500 PICs developed in generic fabs via MPW runs
- There are several key players, mainly in Europe:
  - Silicon photonics: CEA-Leti, IHP, IME, IMEC, VTT
  - InP: FhG/HHI, Oclaro, SMART Photonics
  - TriPleX (SiN): LioniX
  - AIM Photonics won the IP-IMI award in the US
  - And … don’t forget about packaging

Decide on foundry

Foundry platforms - overview

Broker	Process	Lasers	SOAs	TDBR	Modulators / Phase shifters				Detectors			Prop loss
					L (mm)	Vp - Pp	Loss (dB)	B (GHz)	R (A/W)	B (GHz)	I_{dark} (nA)	dB/cm
JePPIX	Oclaro TxRx 10G	YES	YES	YES	1	3.5	< 2	> 10	0.8	10		2-3
JePPIX	HHI Tx- Rx 25G	YES	YES	YES	0.5	(25 mW)	< 2	(kHz)	0.8	40	< 10	1-2
JePPIX	SMART TxRx 10G	YES	YES		2	7	< 2	10	0.8	10	< 20	3-4
JePPIX	TriPleX (DS-500-170)				1-2	(500 mW)	< 0.1	(kHz)				< 0.5
VTT	VTT 3 µm SOI				1		< 0.1	(kHz)				0.1-0.15
Europractice	Imec ISIPP25G+				1.5	7	6	20	0.5	> 50	< 50	1.5-2.5
					0.04*	2*	5*	>50*				
Europractice	CEA-LETI Si310-PHMP2M				1 - 4	< 7.5	<2.5	< 12	0,7	30	< 10	< 2.5
Europractice	IHP											

*Germanium electro absorption modulators

- TriPleX and VTT 3 µm SOI have the lowest losses. TriPleX is also suitable for visible light
- For active components with gain and lasers, only InP can be used
- Silicon for high integration density, reproducibility and volume scalability

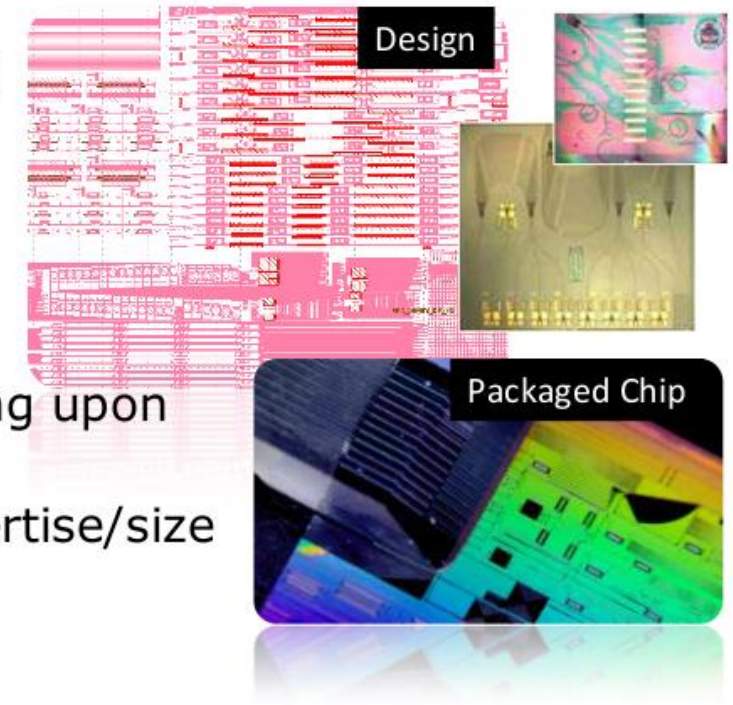
6th European Photonic Integration Forum

Typical timelines

Photonic MPW Development Cycle

- Concept to Design Phase (1-3M)
- Fabrication cycle (2-6M)
- Packaging (1M)
- Testing (1-2M)

Second Iteration (5-10M) depending upon
1. Technology complexity
2. Product development team expertise/size
3. Design experience

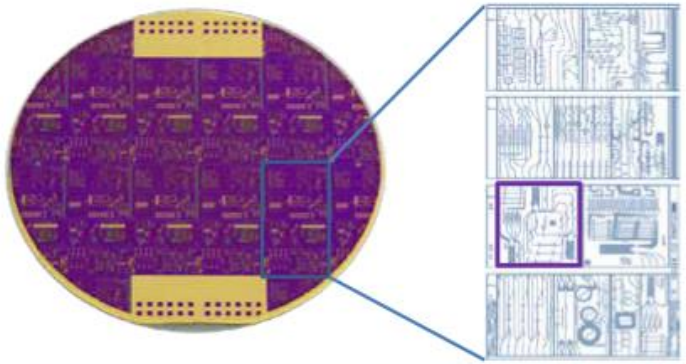


6th European Photonic Integration Forum

Rules of engagement

How to get access?

1. Sign user agreement: NDA
2. Get access to Design Manual and PDK
3. Reserve a cell in one of the MPWs
4. Design using PDK: implemented in software tools
5. Get design support from Design Houses
   or design by yourself
   (PIC training recommended)
6. Send in your design on time



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Source: IBM

PIC Design Software

- Today really good design solutions are available
  - Electronics Design Automation (EDA) made for Electronic ICs
  - Likewise, Photonic Design Automation (PDA) being created for PICs
- But there are in between situations:
  - What if your chip has optical as well as electrical components?
  - What if you plan to do the photonic simulations in PDA, but then use EDA for the mask layout?
  - And, there are ongoing efforts between EDA and PDA providers to make their S/W interoperable and support the industry to scale from R&D to (volume) manufacturing
- Even though some functions can be done using both PDA as well as EDA, some care is needed…

EDA and PDA: photonics ≠ CMOS

Digital IC design flow

Specification
System Design
Circuit Design = Auto-generated

System Simulations

Circuit Layout = Auto-generated
Top-level = Auto-routed
Verification
Manufacturing

RF-IC & Photonics design flow

Specification
System Design
Circuit Design
Component Design
Circuit Simulations
Worst-Case Circuit Simulations
System Simulations
Worst-Case System Simulations
Circuit Layout Design
Top-Level Layout/Interconnect
Verification
Manufacturing

EDA and PDA: photonics ≠ CMOS

Analog design time syndrome
"for a 10% analog 90% digital IC, the analog design takes 90% of the design time"

Circuit Design = Auto-generated

System Simulations

Circuit Layout = Auto-generated
Top-level = Auto-routed
Verification
Manufacturing

Circuit Design
Component Design
Circuit Simulations
Worst-Case Circuit Simulations
System Simulations
Worst-Case System Simulations
Circuit Layout Design
Top-Level Layout/Interconnect
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Manufacturing

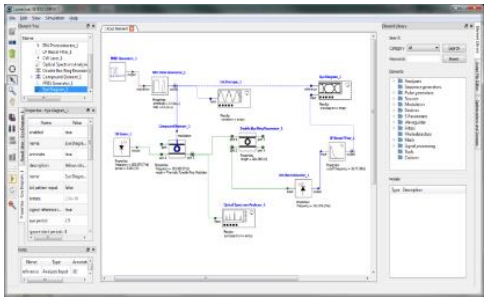
Integrated Photonics Design

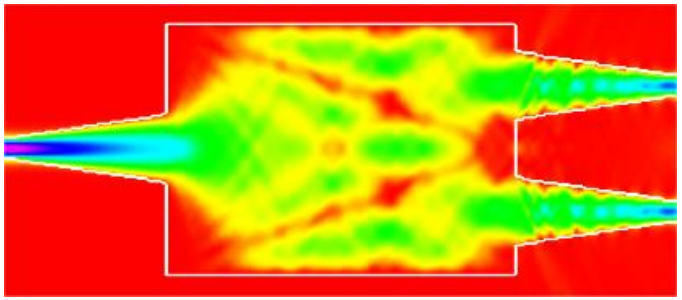
Requires for simulations:

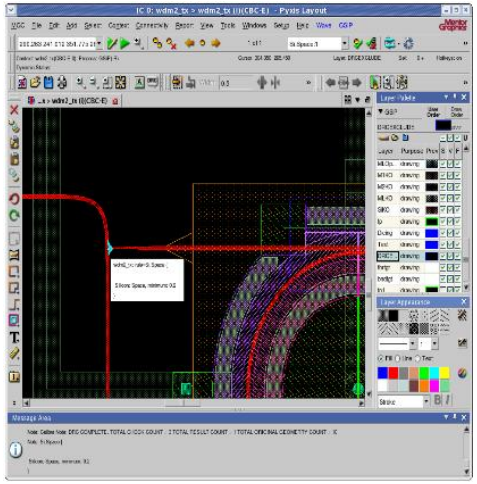
- Dedicated photonic circuit simulation tools
- Special physical simulation tools for integrated photonics
- Interaction between electronics and photonics

Requires for mask layout:

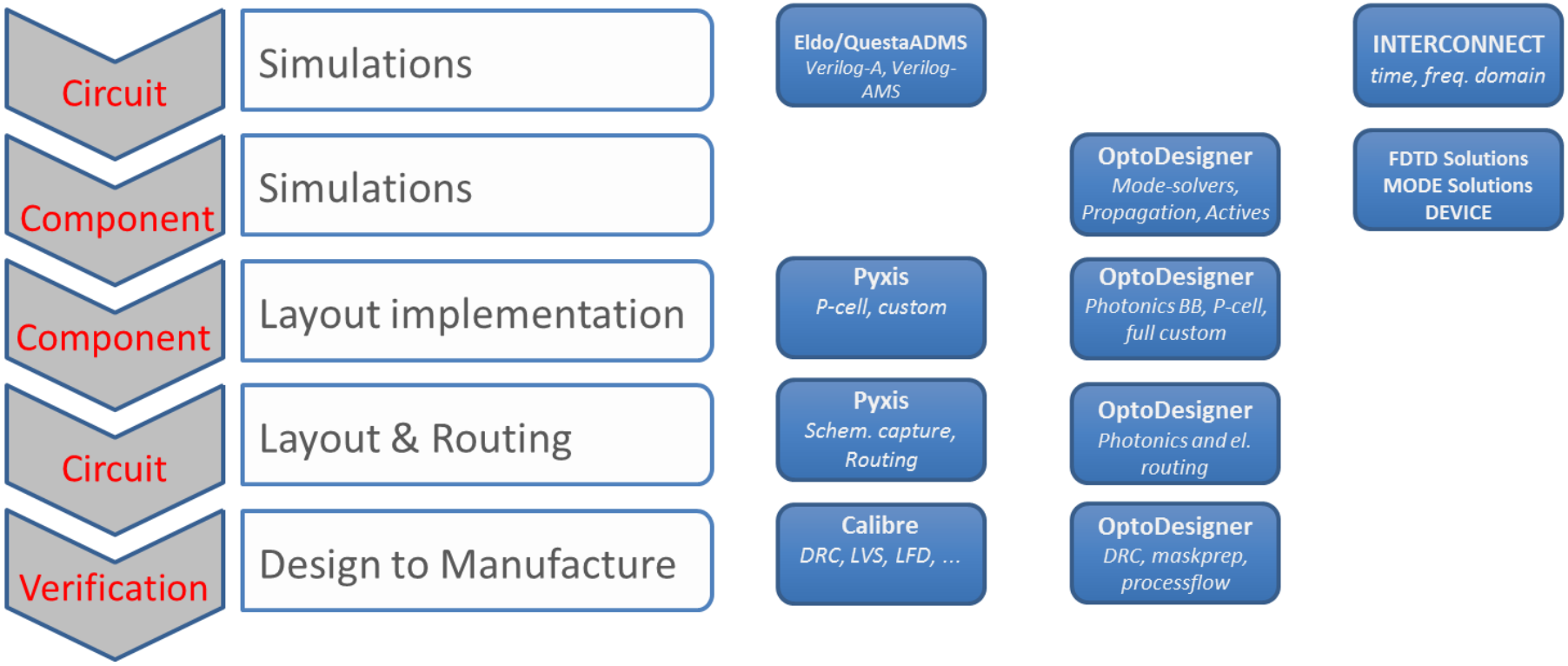
- Accurate and flexible definition of all angle shapes
- Advanced gridding and fracturing of polygons
- P-cell like definition for primitives and compounds
- Special features for verification (DRC, LVS)





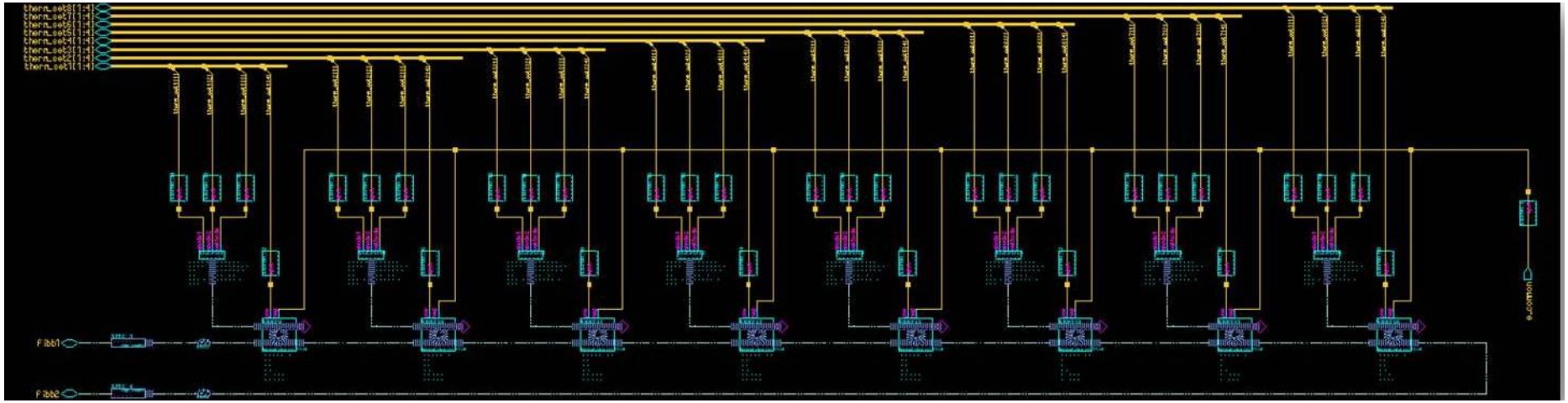


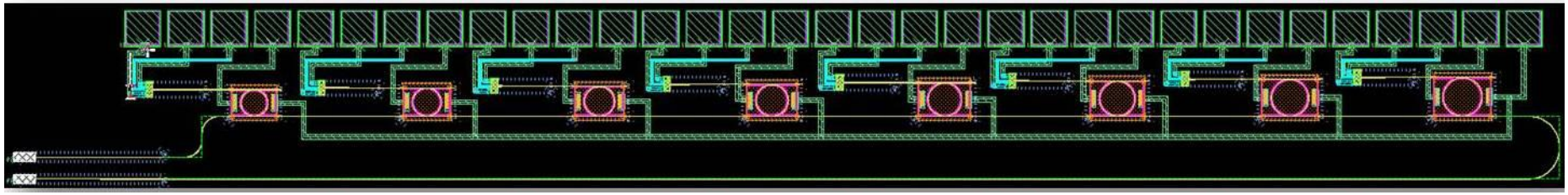
Tools available for full flow



Tools support circuit design

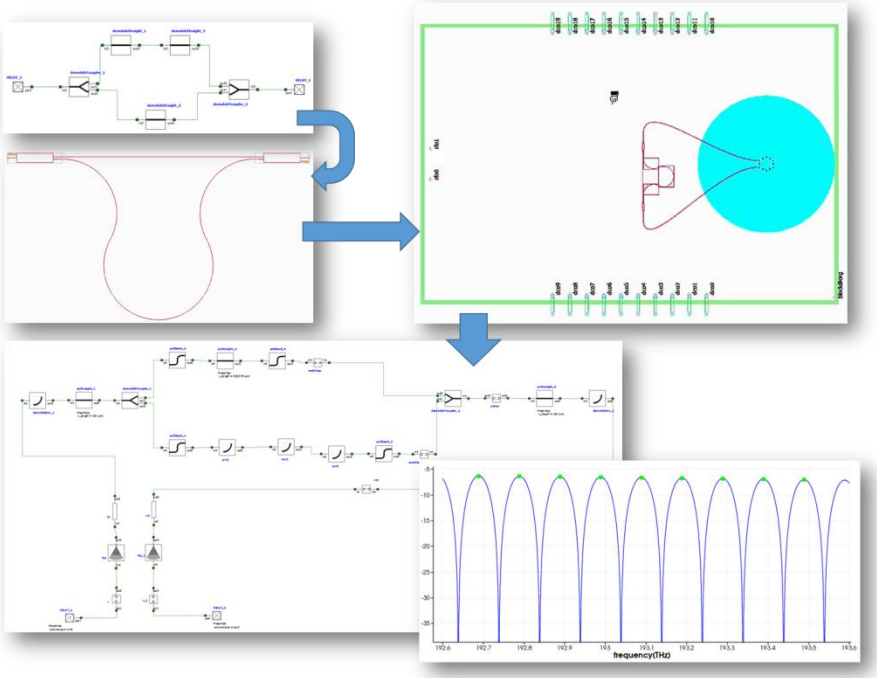
- Pick, place and connect validated components
- Photonic and electrical connections automatically detected
- Schematic connectivity will drive layout directly

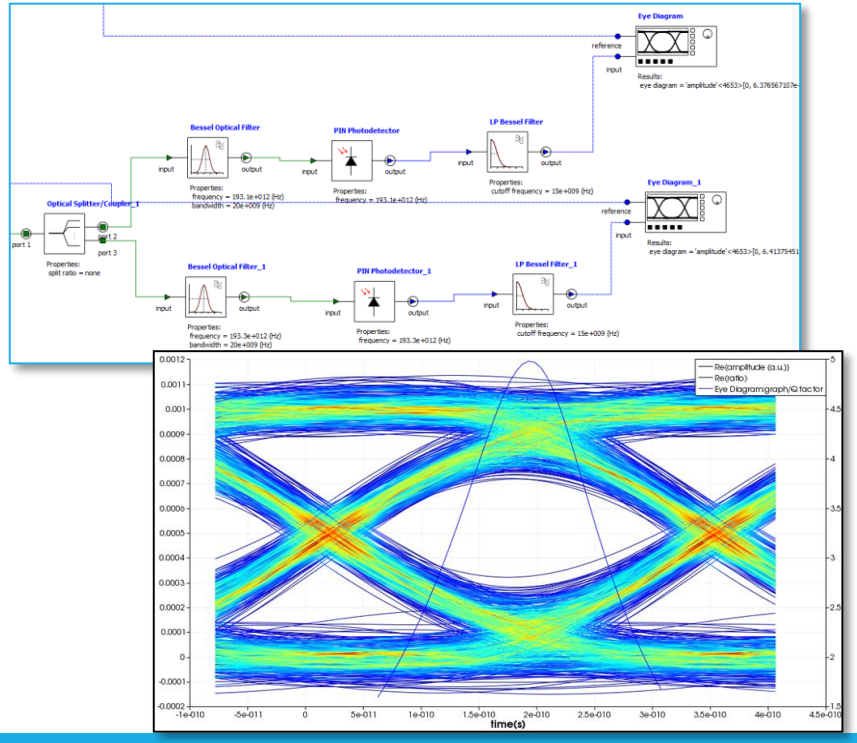




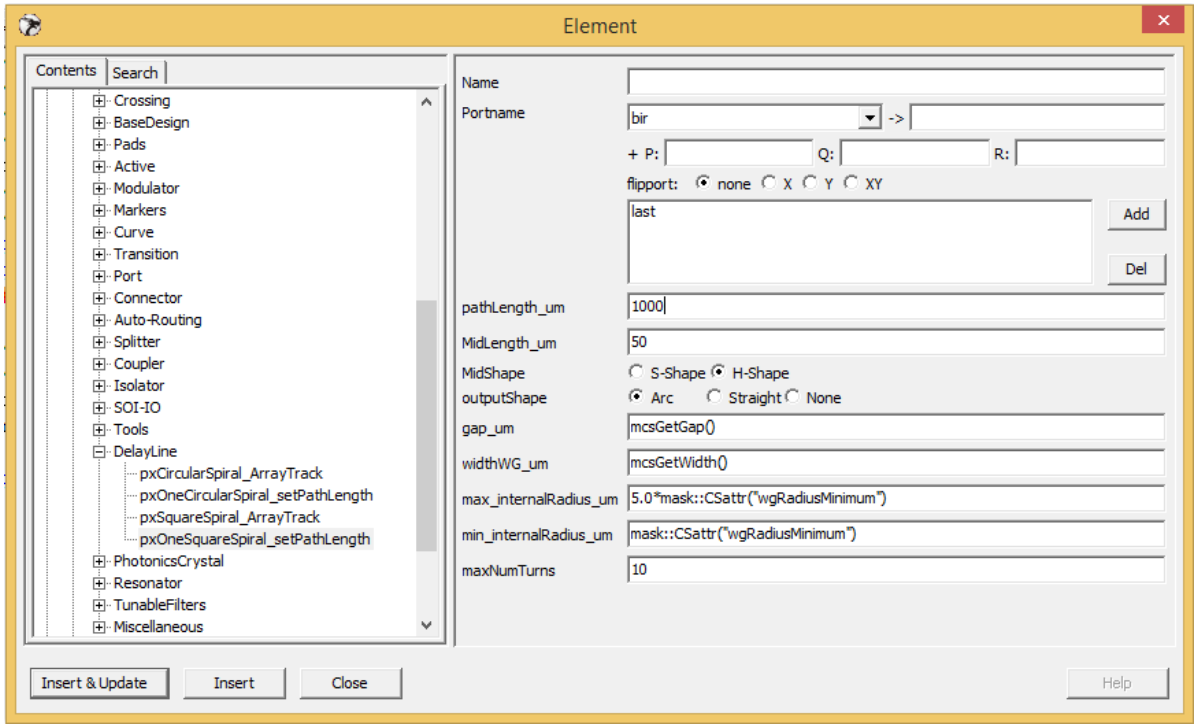
Tools support circuit simulations

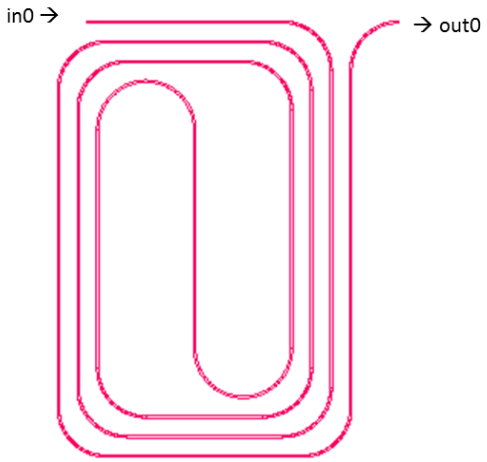
- Calibrated model libraries improve design accuracy
  - Design using compact model libraries of fundamental and complex devices, calibrated to foundry processes
  - Frequency & time domain simulation





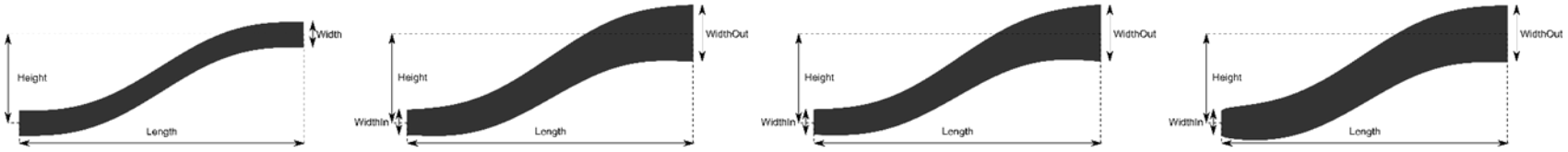
Tools support component design





Spiral delay-line, defined by either geometrical or optical parameters

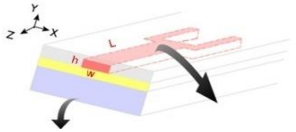
Wide variety of layout primitives available to design custom components, like a parametrized sine-bend

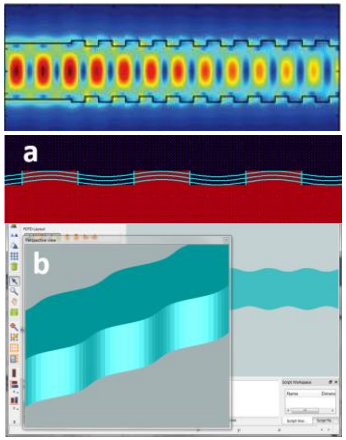


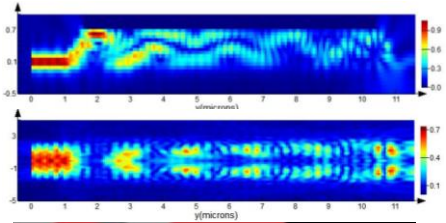
wfix *wlin* *wexp* *wpar*

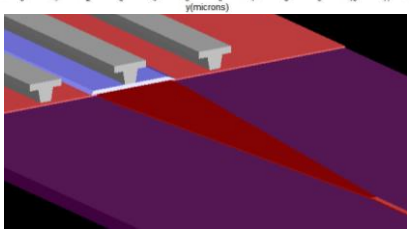
Tools support component simulations

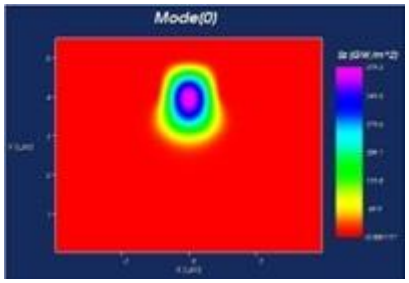
- Propagation simulations: eg. FDTD, EME, BPM
- Mode simulations: eg. mode-solvers, CMT

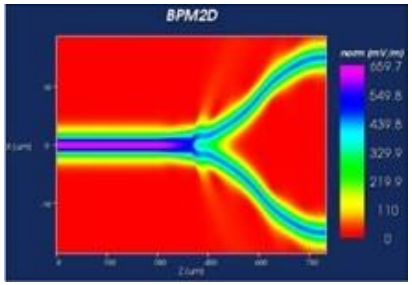


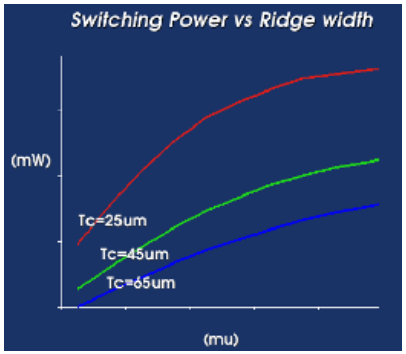


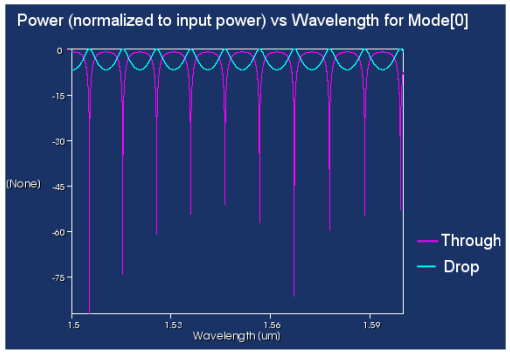


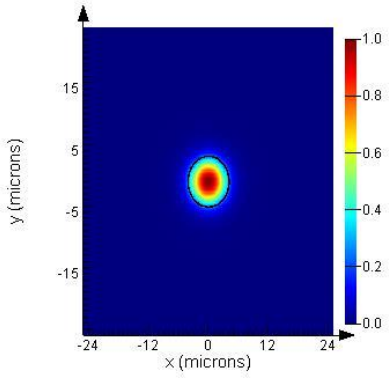


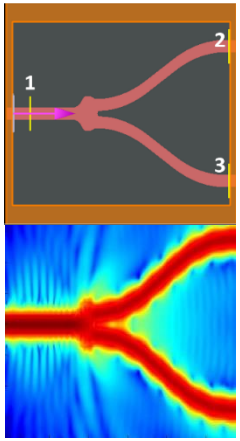






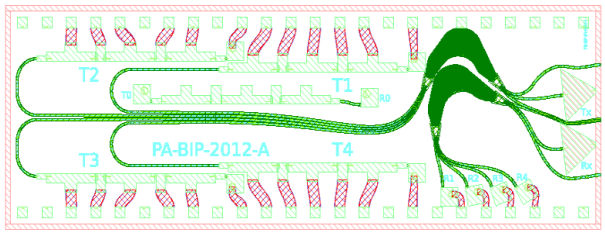


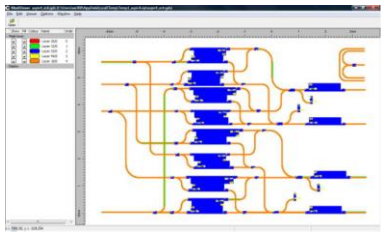


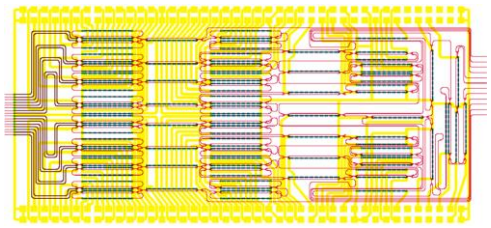


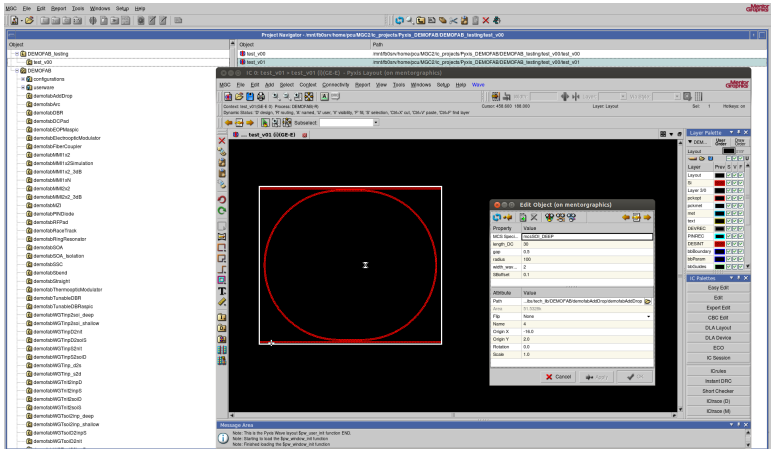
Tools support circuit mask layout

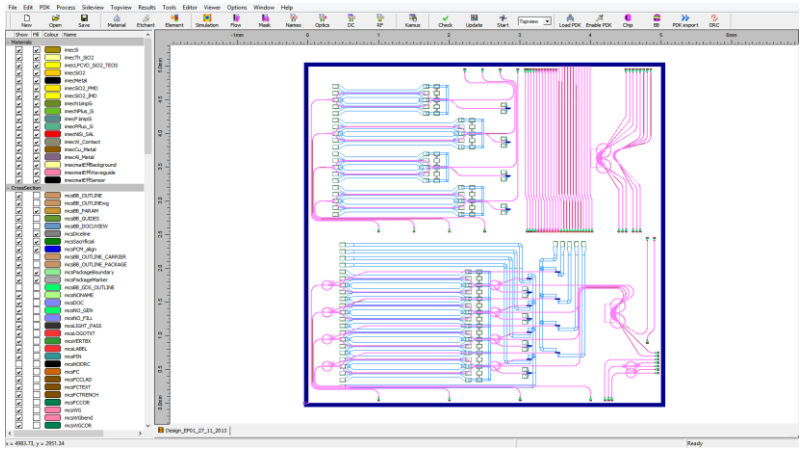
- Pick, place and route or schematic driven layout

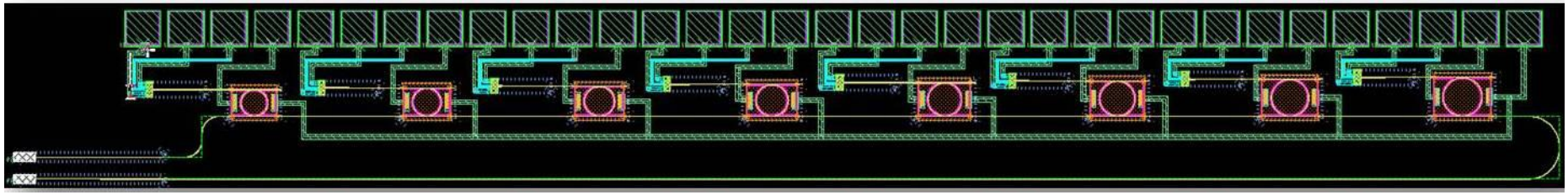








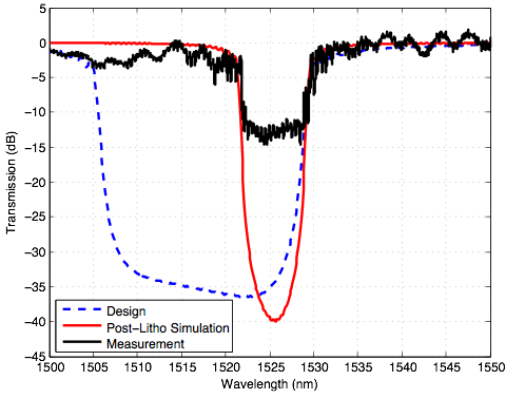




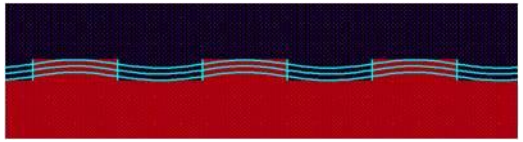
Tools support mask layout

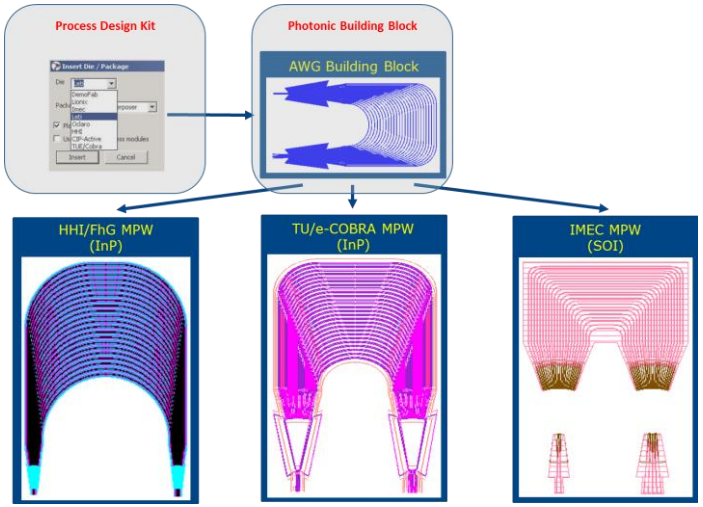
- Design software can translate design intent into layout
- … and correct for process influences

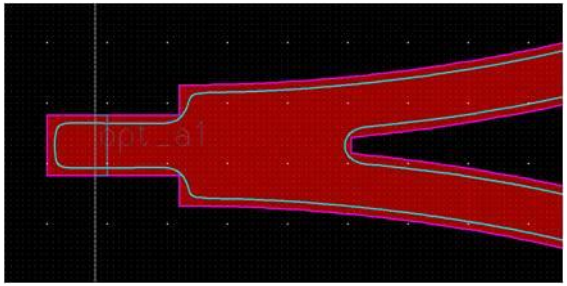
Simulating lithography influence on design intent



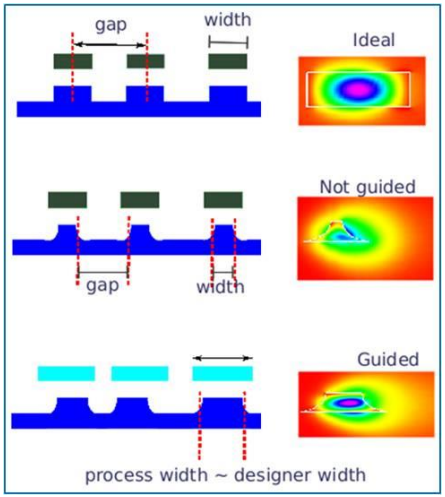
Xu Wang, et al., "Lithography Simulation for the Fabrication of Silicon Photonic Devices with Deep-Ultraviolet Lithography", IEEE GFP, 2012





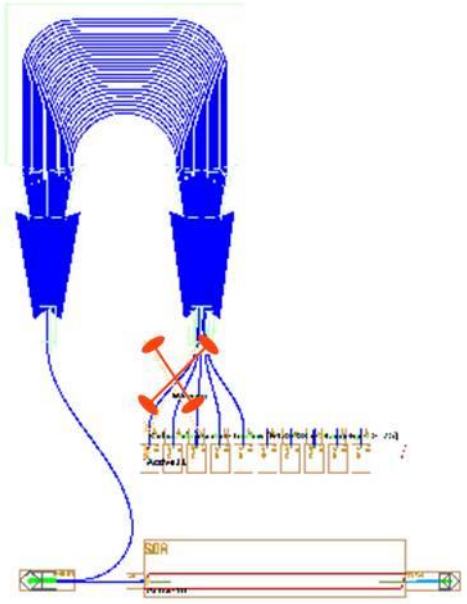


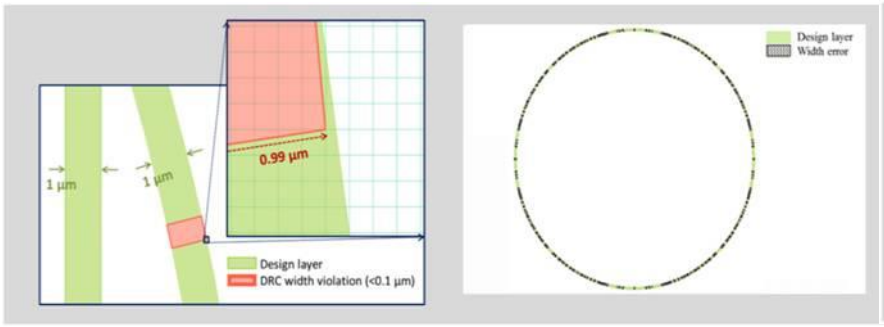
Use technology information to obtain design intent after fabrication

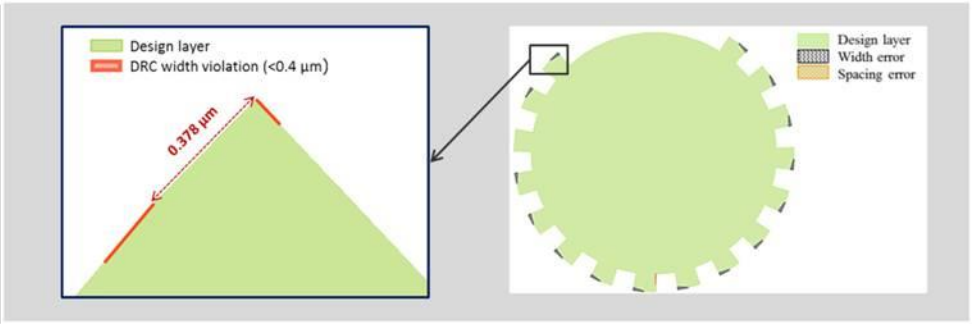


Tools support verification

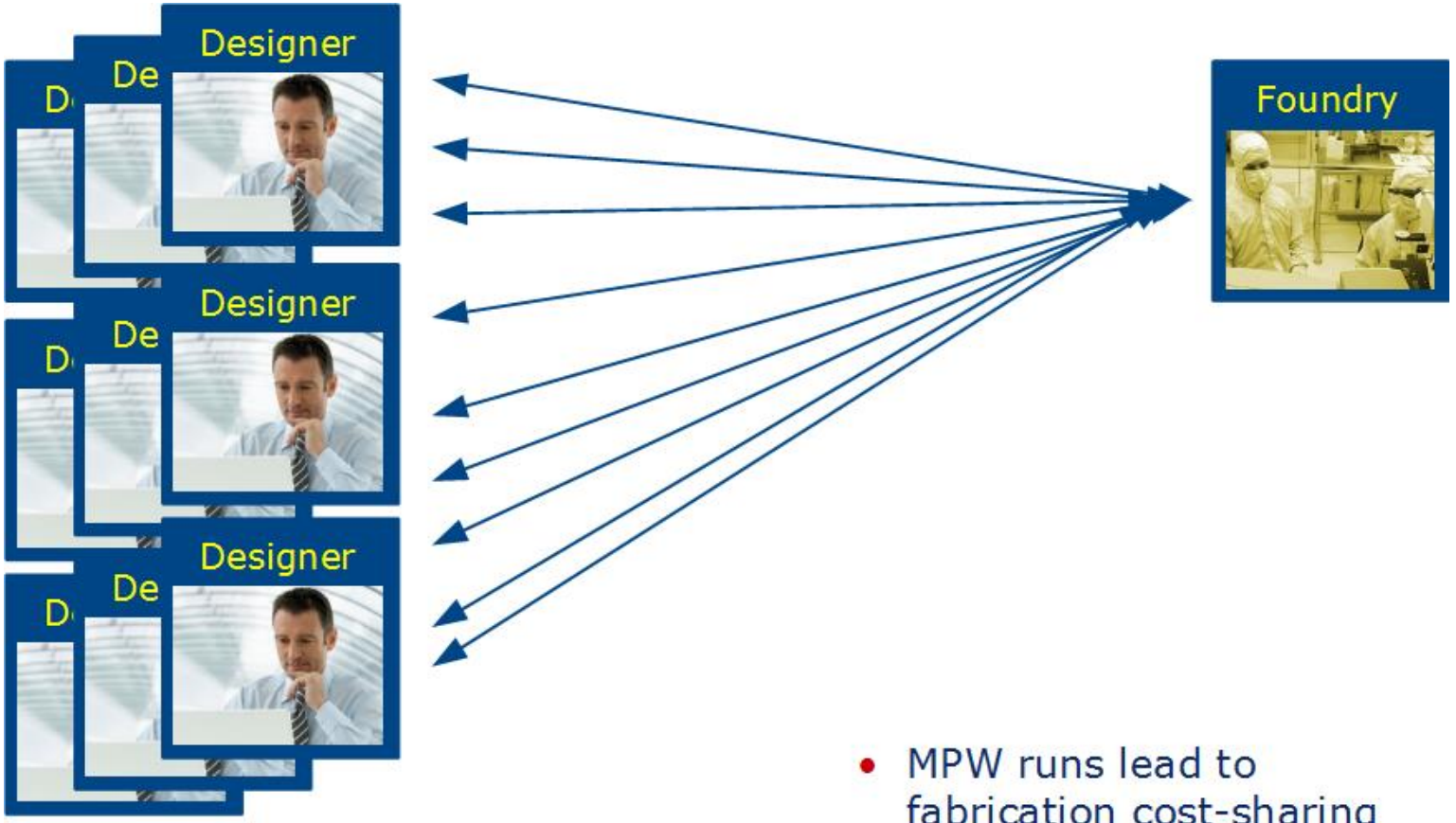
- Functional verification, Design Rule Checking (DRC) and Layout vs Schematic (LVS)
- Built-in photonics relevant design checks (like minimum bend radius)
- Design rules targeting CMOS processes will flag thousands of false errors in photonic structures, Photonic specific DRC rules can minimize false errors
- Integrated design flows enable LVS





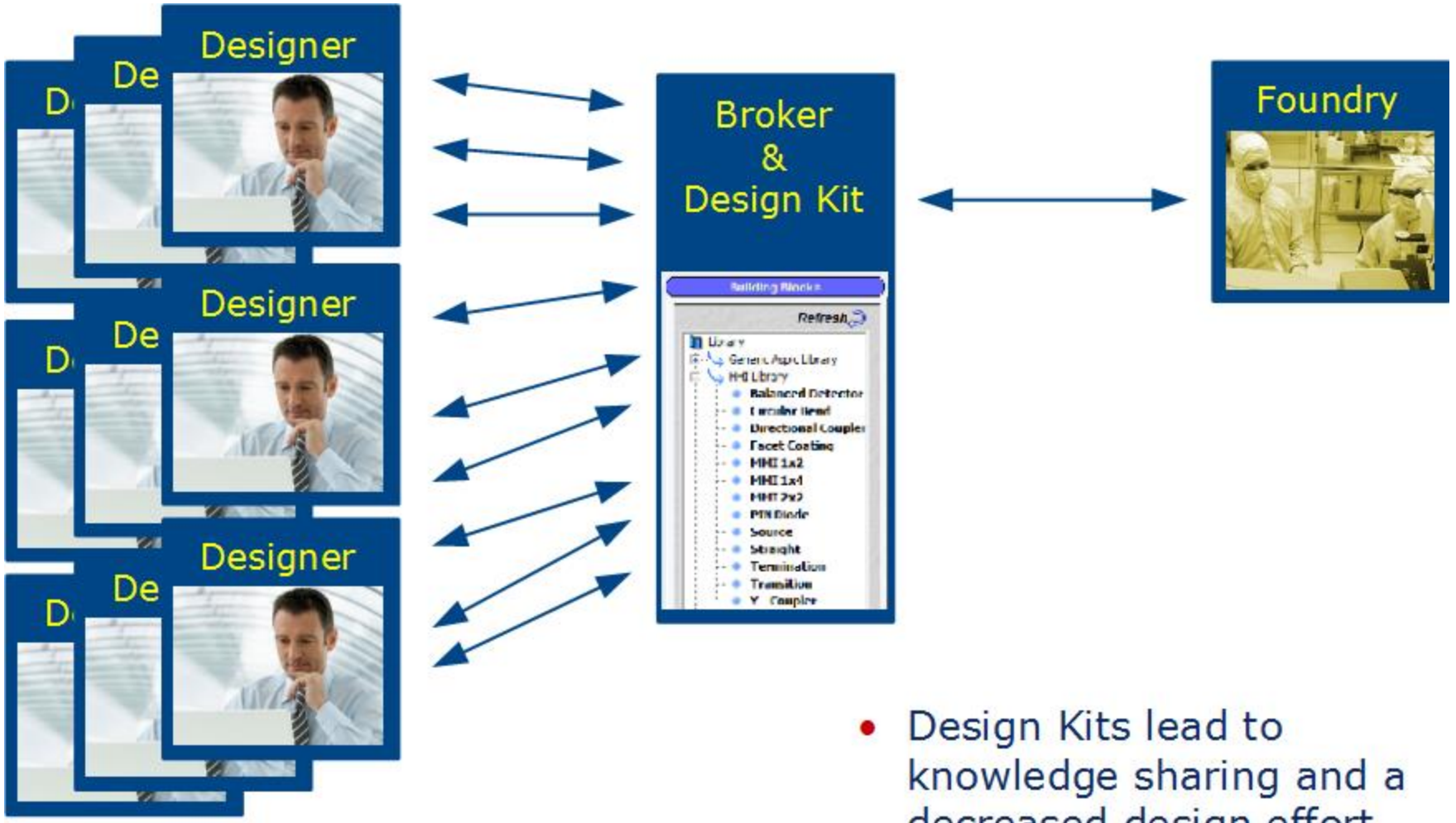


Why are PDKs so important?



- MPW runs lead to fabrication cost-sharing

Why are PDKs so important?



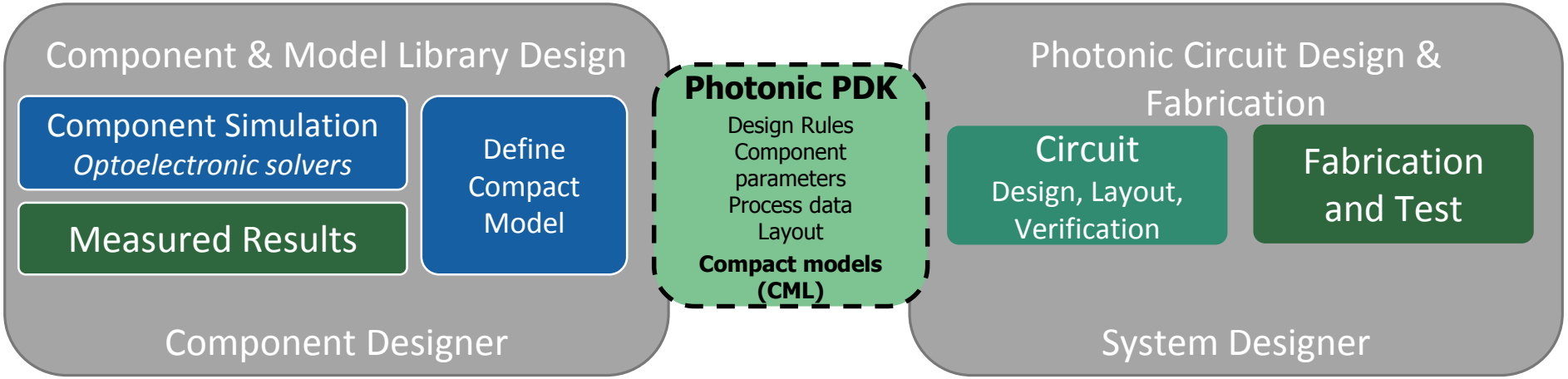
- Design Kits lead to knowledge sharing and a decreased design effort

Why are PDKs so important?

- When working with a foundry (or your own fab), you do not want to reinvent the wheel nor make unnecessary mistakes
  - So all relevant knowledge should be available when designing a PIC
  - And the PDK should be automated (rather than in the form of docs)
  - Without a PDK, there are simply too many unneeded iterations
- What does a PDK include?
  - Design rules and mask layer information
  - Library of validated components
  - Layout information
  - Simulation models and settings
  - Die and package templates

PDKs enable efficient development

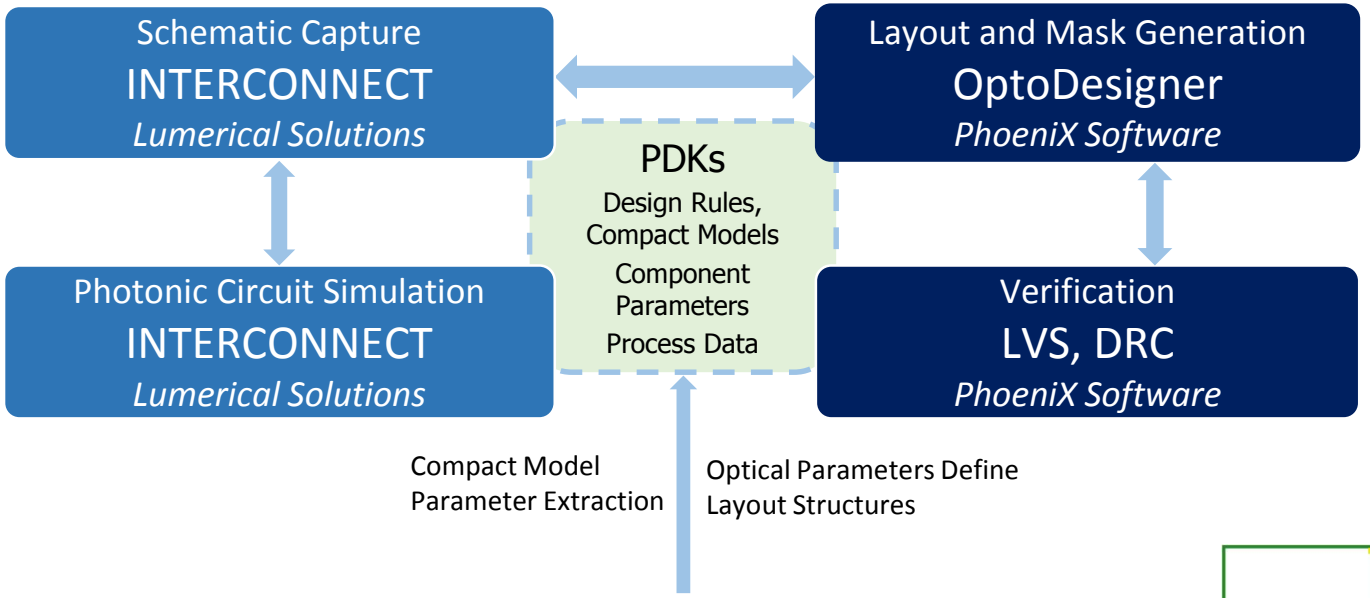
- Faster design cycles and first-time-right designs
  - Higher accuracy by using validated compact model libraries for circuit design
  - Faster layout implementation by using predefined parametric components
  - Higher yield in manufacturing by applying design rules

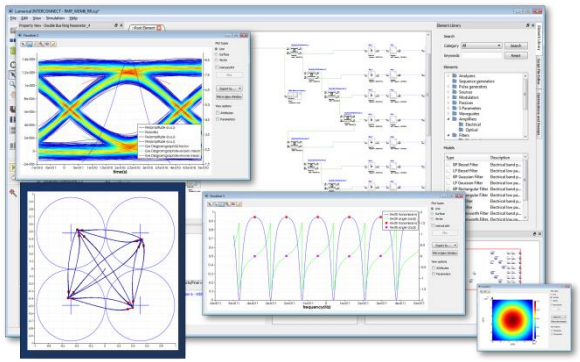


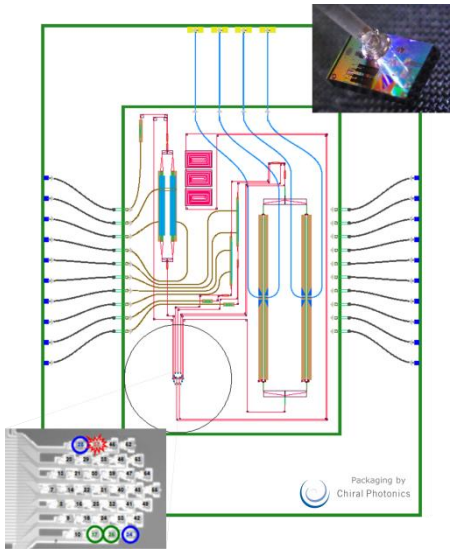
A wide variety of PDKs is available

- Foundries:
  - Silicon: IMEC, CEA-Leti, VTT, IHP and IME
  - InP: FhG/HHI, Oclaro and SMART Photonics
  - TriPleX (SiN): LioniX
- Packaging: Technobis ipps, Chiral Photonics, Gooch and Housego, Linkra, XiO Photonics and Tyndall
- PDKs are available to a varying degree of maturity
- PDKs are typically made available through MPW brokers

PDKs support integration of design flows







PhoeniX Software
Solutions for Micro and Nano Technologies

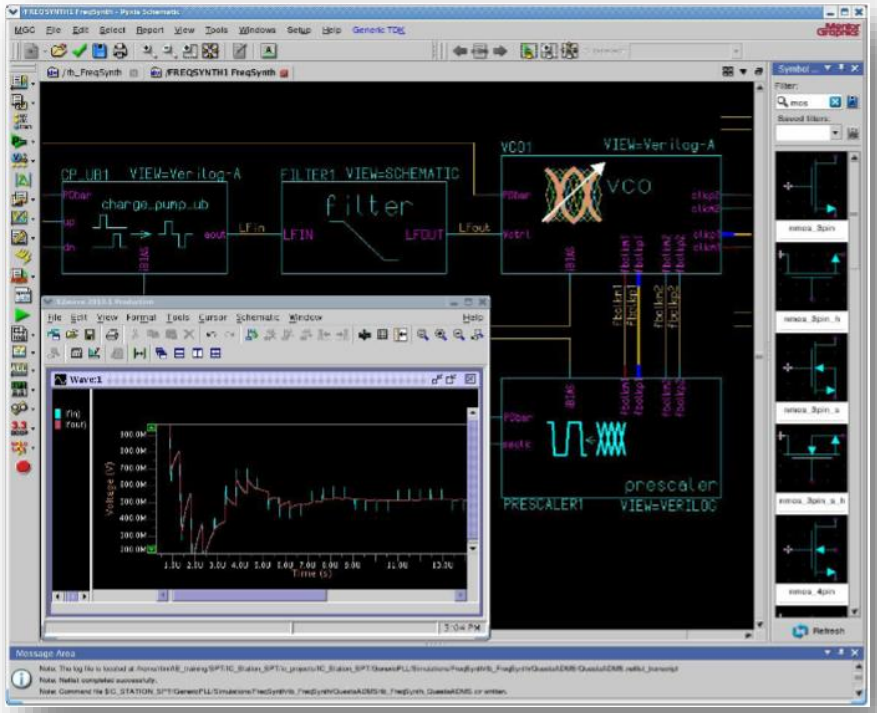
Scaling photonics design

As in the electronic IC ecosystem, faster and more complex photonic ICs will require multi-user collaboration

Innovators will need to build teams with dedicated expertise in multiple areas of PIC design – from system concept to physical layout

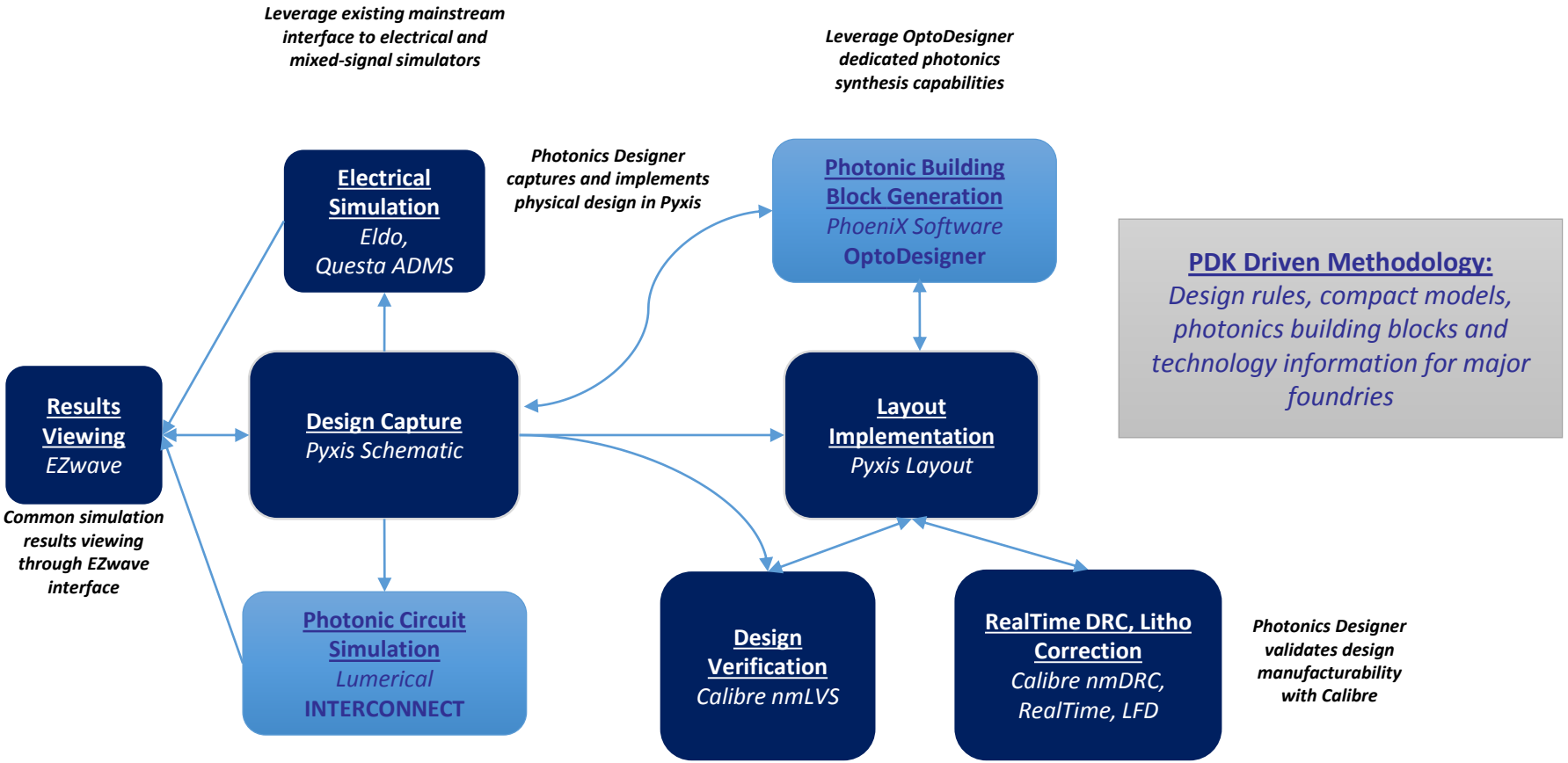
Mentor Graphics provides the tools to do this:

- Pyxis enables multi-user collaboration in common environment
- Calibre provides sign-off assurance through physical verification



Mentor Graphics®

EDA Driven Design Flow



Mentor Graphics®

lumerical

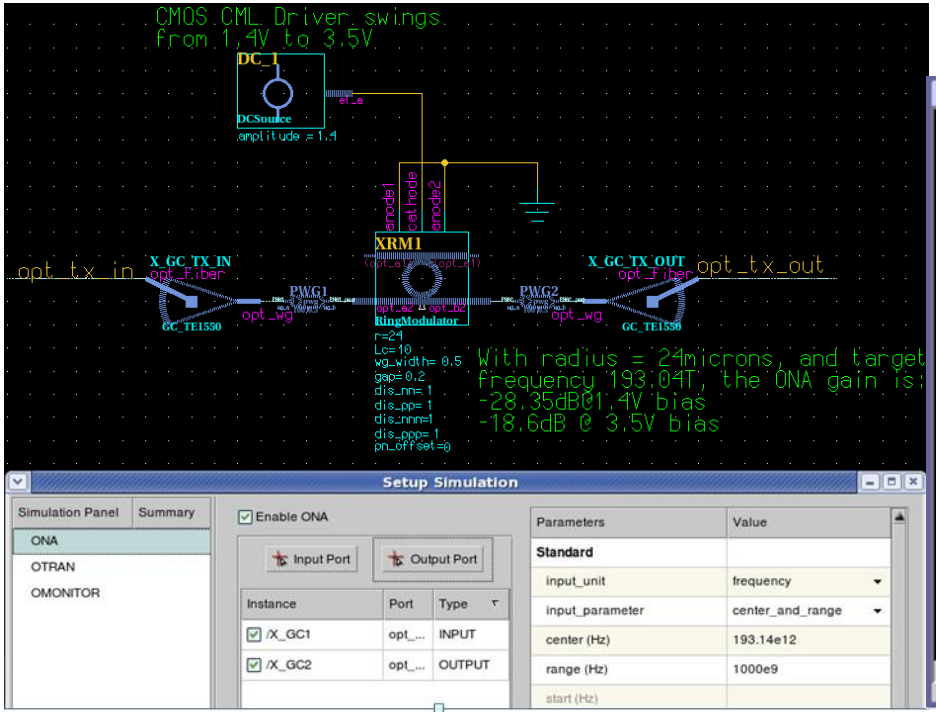
PhoeniX Software
Solutions for Micro and Nano Technologies

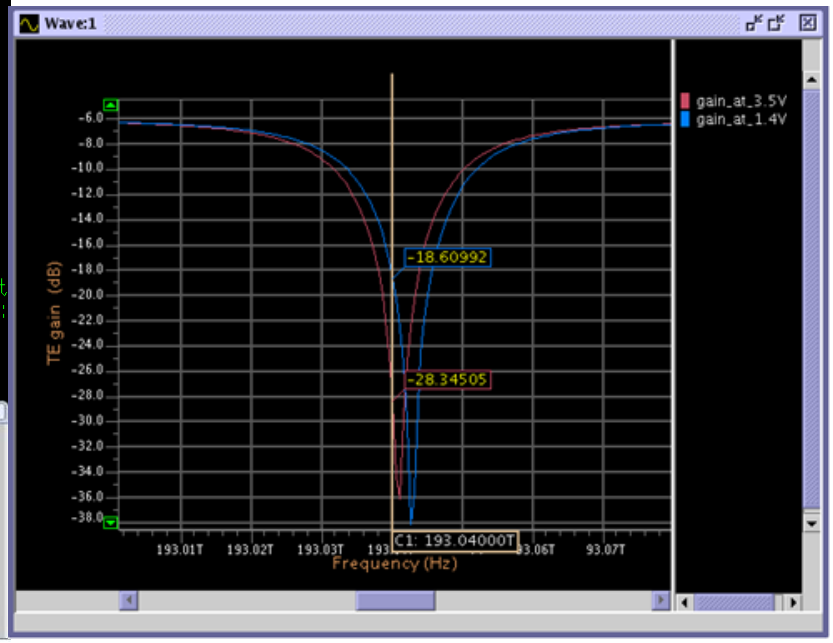
Driving INTERCONNECT from Pyxis

Schematic driven design and simulation

- Interactively setup sizing and DC biasing of modulators in *Pyxis* with *INTERCONNECT* ONA simulation
- View results in *EZwave* results viewer

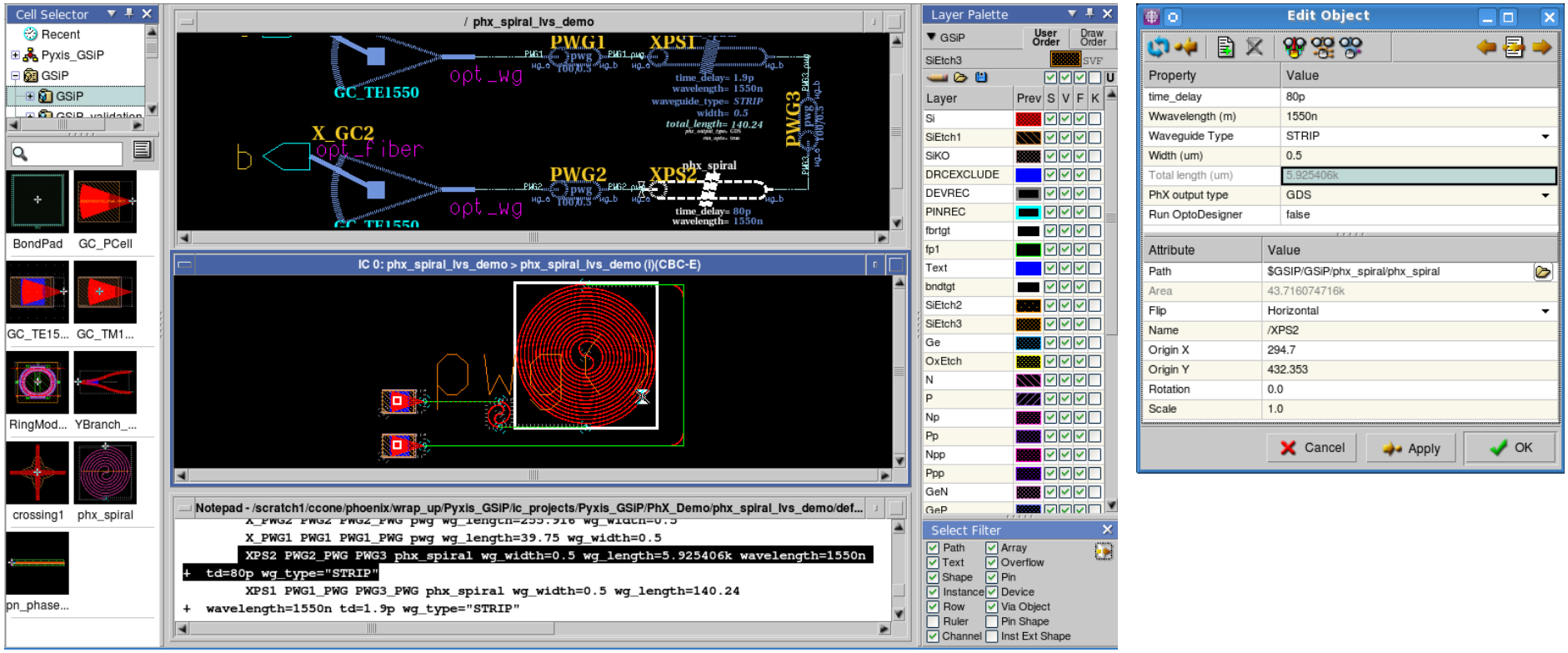
Example: frequency domain spectral response





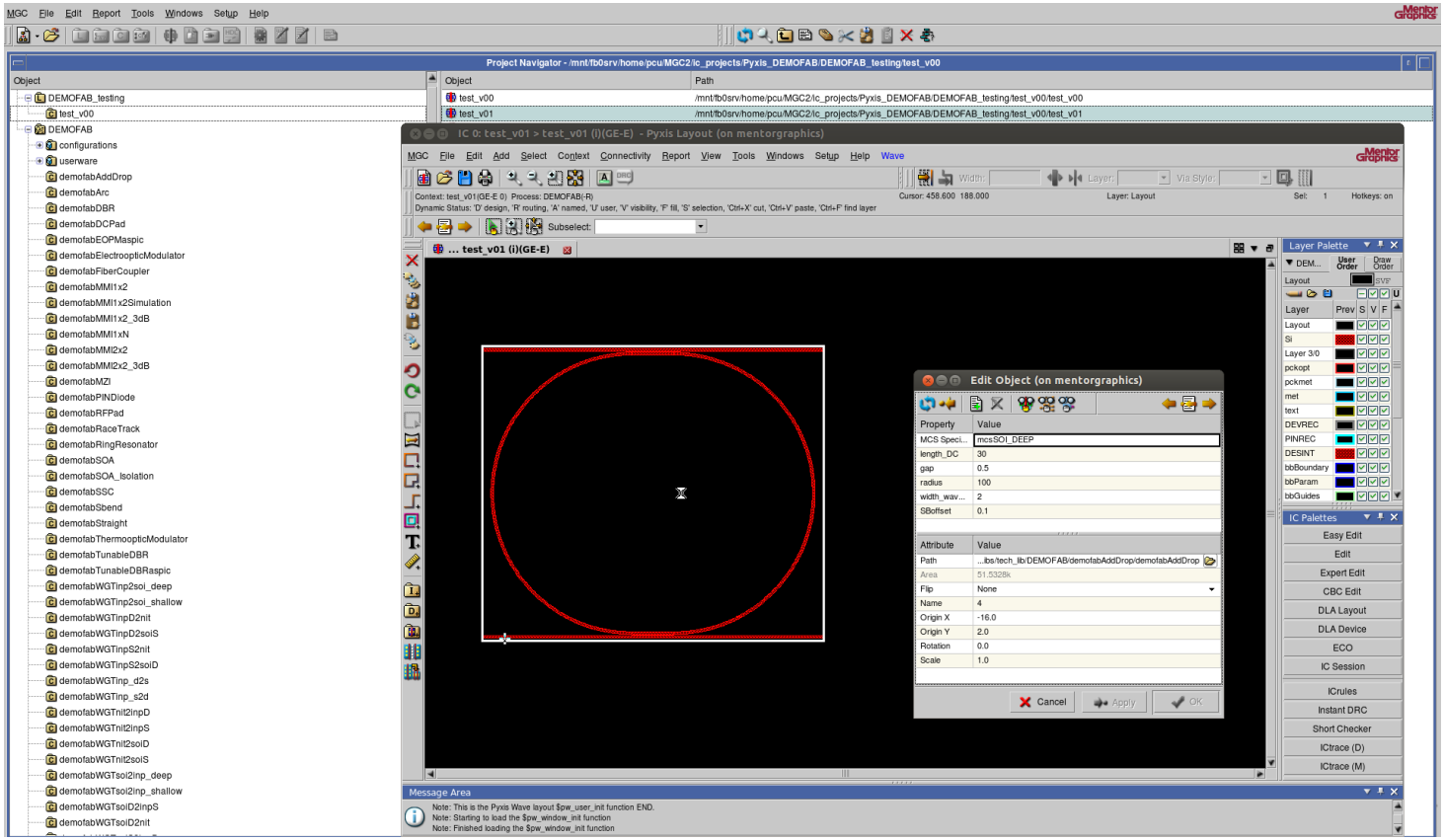
Driving OptoDesigner from Pyxis

- Driving *OptoDesigner* from *Pyxis Schematic* and *Pyxis Layout* to calculate optical parameters and provide layout implementation



Driving OptoDesigner from Pyxis

- All the design elements from *OptoDesigner* are provided in the *Pyxis* environment



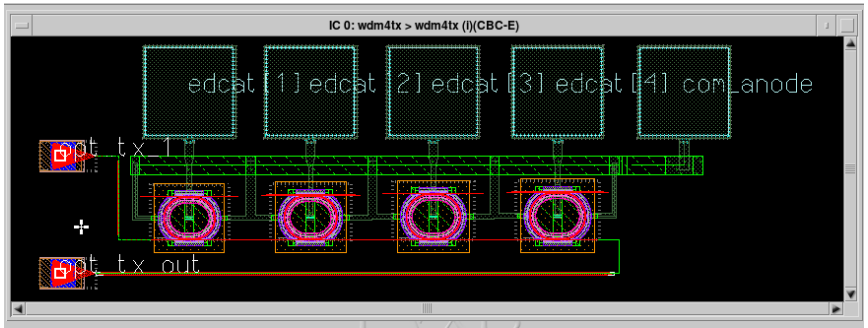
Why Pyxis?

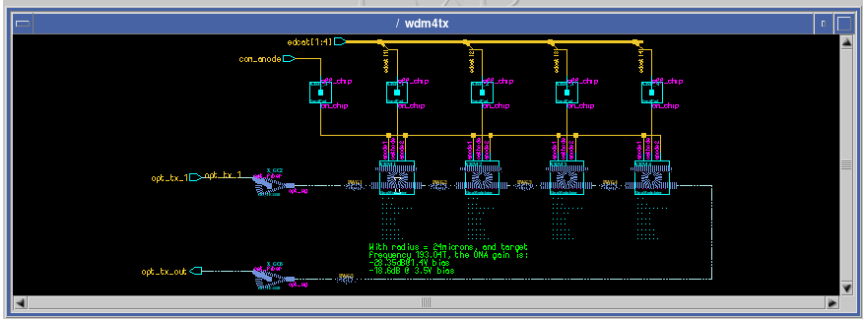
Provides a collaborative multi-user environment

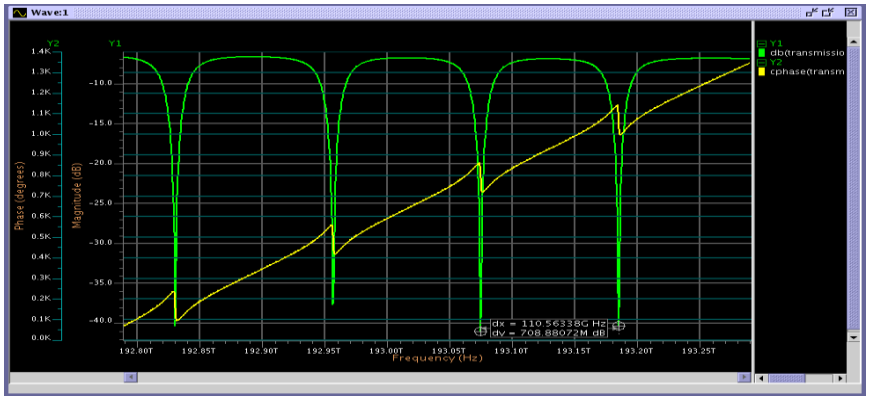
Simulate schematics using Lumerical INTERCONNECT, Eldo with Verilog-A, or Questa ADMS

Flexible infrastructure allows quick integration to any tool accessible within Linux

Complete PDK driven design flow leveraging Calibre, Lumerical and PhoeniX Software







Why Calibre?

Market and industry standard

Fast and accurate DRC:

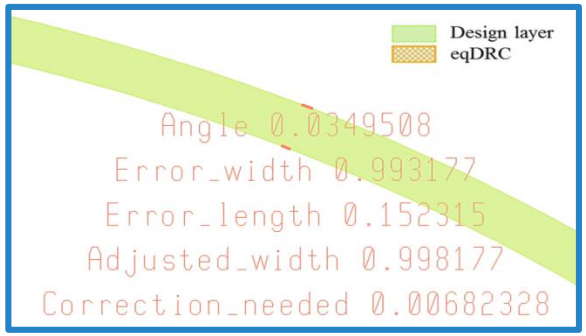
- EqDRC handles complex curves
- RealTime results in Pyxis

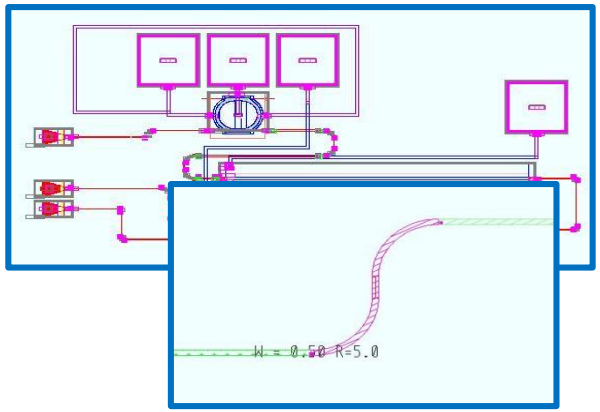
Photonic LVS:

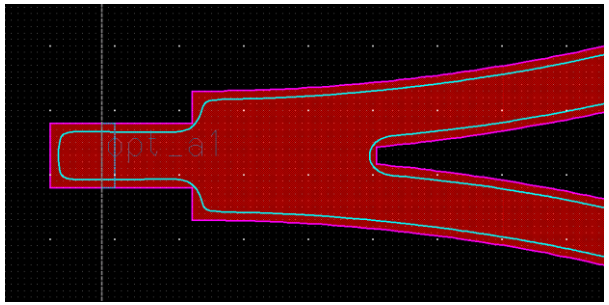
- Shorts & opens detection
- Device validation
- Waveguide interconnect parameter extraction

Lithographic Modeling:

- Reduces manufacture iterations
- Drive accurate photonic simulation





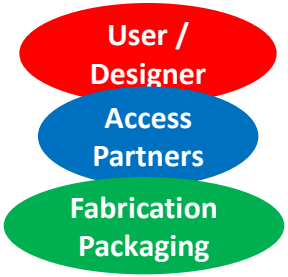


Why Lumerical?

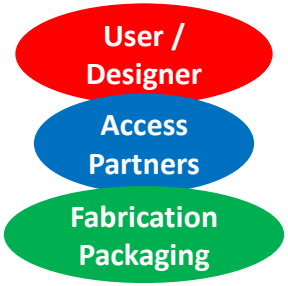
Three Distinct Design Activities for PIC Development

1. Component-level design and optimization
   - Design and optimize a component for desired performance

2. Compact model library generation for PDKs
   - Build compact model for component
   - Calibrate against experimental results
   - Inform with simulation results



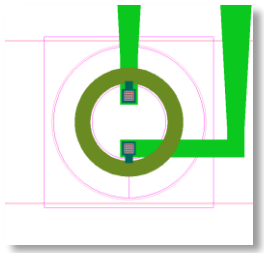
3. Photonic Integrated Circuit design and optimization
   - Build complex circuits based on known components with validated compact models

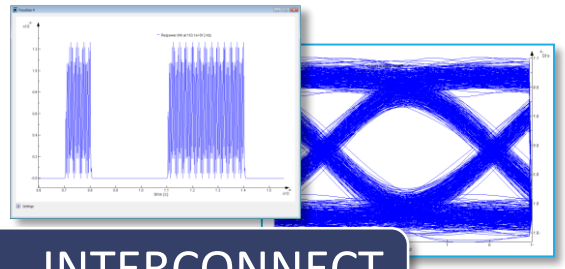


Why Lumerical?

PDKs
Design Rules,
Compact Models
Component
Parameters
Process Data

Layout Information
Process Information
Design Rules





INTERCONNECT
Photonic Integrated Circuit
Simulator

Compact Model Library for
Circuit Design &
Optimization

Photonic Component Design
Optoelectronic Solvers,
Experimental Data

Compact Model
Parameter Extraction

FDTD Solutions
Nanophotonic Solver
(2D/3D)

MODE Solutions
Waveguide Design
Environment

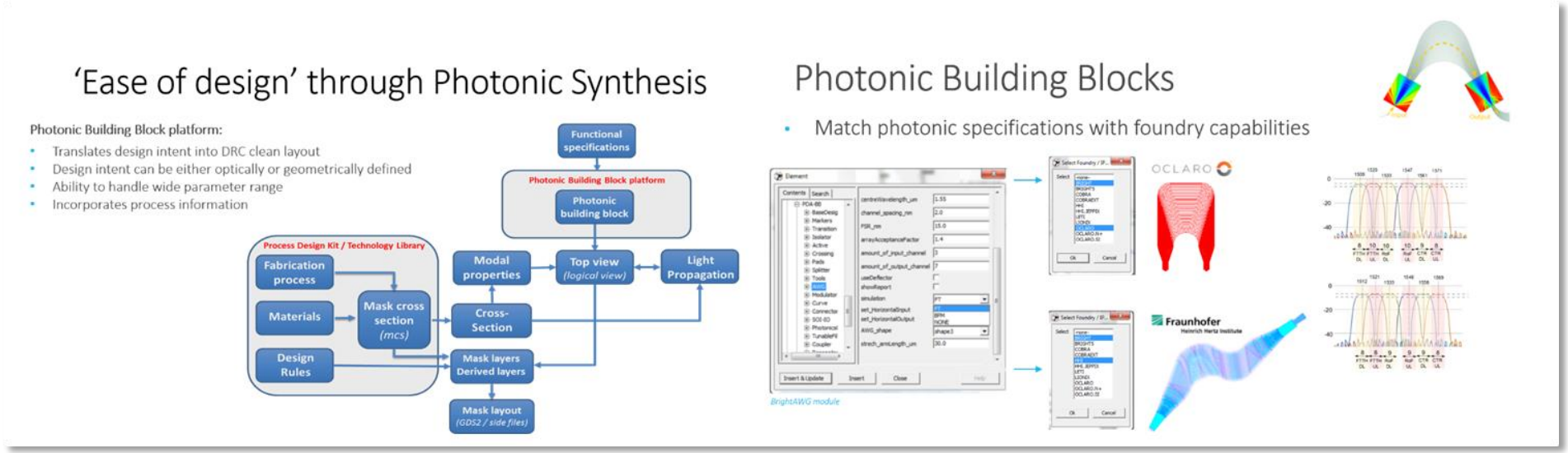
DEVICE
Charge Transport
Solver (2D/3D)

- Parameter Extraction for Compact Models
- Component Design & Optimization

Why PhoeniX Software?

PhoeniX Software
Solutions for Micro and Nano Technologies

- Focus on Design for Manufacturability
- We have been supporting 100's of designers (MPW-users and at vertically integrated organizations) getting started with PIC design
- More than 25 years photonics design and tools expertise, available trough excellent customer support
  - Our support is valued by our customers with a 9.1 out of 10

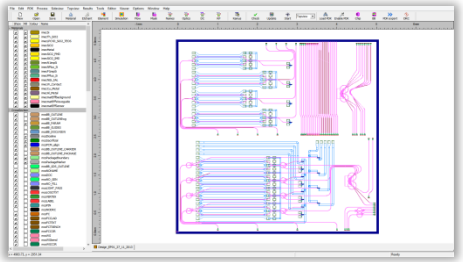


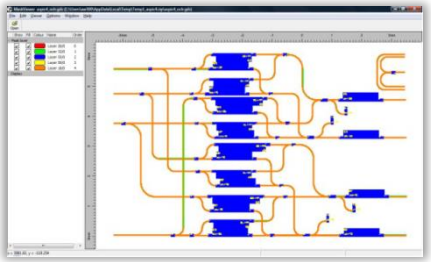
Why OptoDesigner?

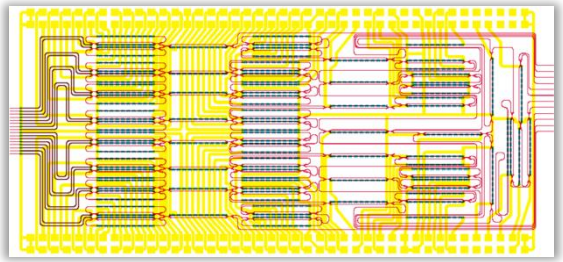
PhoeniX Software
Solutions for Micro and Nano Technologies

- Native all-angle and all-shape design
- Complete parametrized library for photonics
- Includes photonics verification and design rule checking
- Interfaces with world-class 3rd party circuit simulators
- Enables EDA centric design flows
- Easy to use GUI including powerful scripting
- PDKs available for 8 photonics foundry services

More than 300 designs created and fabricated in MPW's in the last 3 years!







Further Information

www.lumerical.com

More material including demo movies for the EDA-style design flow: www.lumerical.com/tcad-products/interconnect/pyxis_eda/

And for the INTERCONNECT – OptoDesigner interface: www.lumerical.com/phoenix/

www.mentor.com

A generic, non-proprietary silicon photonics design kit is available for download at www.siepic.ubc.ca/GSiP

www.phoenixbv.com/optodesigner

Overview of available PDKs: www.phoenixbv.com/designkits