MOSIS Service
Silicon Photonics MPW Access

Russ Piña
Nankyung (Nan) Cockerham
Multi-Project Wafer Service

Many designs on single die; cost to customer is approximately in direct proportion to area used.

Shared costs: mask, wafer, and foundry and packager interface

~ 50 different designs

Your Chip Is Here

Multi-project reticle
History and Capabilities

- Started by DARPA in 1981, to reduce the costs of prototype fabrication to their research community
  - Over 60,000 user designs managed
- Capabilities
  - People: *Dedicated team for design, layout, test, packaging, modeling, customer support, etc.*
  - Test lab: *Parametric test systems, 200 mm and 300 mm fully automated wafer probers, etc.*
  - Computing: *High-capacity servers for design checking, pre-fabrication processing*
  - Software: *Automated 24/7 web-based design submission and fully automated layout checking, project status tracking*
MOSIS: Low-Cost Semiconductor Prototyping and Small-Volume Production Service

Low-Volume Circuit Designers
-- Startup, Commercial, Defense, University, etc.

MOSIS provides all these services to the Integrated Circuit design and fabrication community with integrated seamless interfaces

- Circuit Designs
  - Design Kits, Doc
  - Design Check
  - Technical Q’s
  - Prototypes/Small Prod.
  - Flexibility on Die Size

- User Support
  - Since 1981
  - ITAR – USA Vendors
  - DMEA Accredited/Trusted
  - > 60,000 Completed Projects

- Cost-Effective Prototype and Small-Volume Chips

- Leading Foundry Access
  - Small Lots, Multi-Project Runs
  - TSMC, Global Foundries, …
  - CMOS, RFSoI, SiGe, Photonics

- Process Monitoring
  - In situ circuits

- Wafer + Device Testing
  - Parametric, Functional

- Dicing + Packaging
  - Flip-Chip, Plastic, …

USC Viterbi
School of Engineering
MOSIS Customer Base

- Large/Medium Size firms (Fabless or IDMs)
  - Require leading-edge technologies not available in house
  - Require low-cost prototyping option

- Fabless semiconductor startups
  - Limited financial resources
  - Emerging market sectors requiring leading edge technologies

- Companies with DoD funding
  - Require leading-edge technologies, with USA source
  - Optional support for ITAR, Trusted designs

- Universities
  - Research and education
Current Foundry Partners

MOSIS

TSMC

GLOBALFOUNDRIES

IMEC

austria microsystems

ON Semiconductor

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School of Engineering
Silicon Photonics MPW Service

- In-House Expertise in Silicon Photonics
- Involvement in U.S. National Photonics Activities
- Quick Response to Design Submission Issues
- U.S. Based
  - Support During U.S. Work Day
  - Simplified PO Process
IMEC Design Kit Access

- MOSIS Customer Account
- Submit Vendor Document Access
- Complete MOSIS-imec DKLA
- Access Design Kit via MOSIS
- Secure Document Server
Process Options

**ISIPP25G+**:
- Each order includes 20 duplicate dies
- Extra dies can be purchased
- Choice of implants
- User metrology

**PSV**:
- Each order includes 25 duplicate dies
- Extra dies can be purchased
- Choice of cladding (top oxide, side oxide, air)
- Choice of Lithography dose (standard, high)
- User metrology
MPW Runs 2015

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<tr>
<th>Technology</th>
<th>ISIPP25G+</th>
<th>PSV</th>
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<tr>
<td>Registration</td>
<td>19-Oct-15</td>
<td>16-Nov-15</td>
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<td>DRC clean Deadline</td>
<td>16-Nov-15</td>
<td>30-Nov-15</td>
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<tr>
<td>Estimated Ship Date</td>
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<td>April 2016</td>
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Refer to MOSIS website for updates and status of these MPW runs:
https://www.mosis.com/vendors/view/imec
MOSIS Contact Information

- Website: www.mosis.com
- Contacts:
  - Wes Hansford, Director
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- Customer Support
  - https://www.mosis.com/pages/account-login
GFUS 7RFSOI for Photonics IC

Nan Cockerham – MOSIS
October 2015
Options for Silicon Photonics

- Heterogeneous: III-V Actives + Silicon Passives
  - Leverage advantages of both processes

- Hybrid: Specialized SOI process without Electronics
  - Si photonics process offered by IMEC and IME

- Monolithic: Specialized SOI process with Electronics
  - 90 nm CMOS9WG process

- Standard SOI CMOS
  - GFUS (formerly IBM) 45 nm and 32 nm SOI process
  - GFUS (formerly IBM) 180 nm 7RFSOI process
GF CSOI7RF Process Overview

- **CSOI7RF Technology Details**
  - 180 nm CMOS7RF based SOI technology
  - 7RF 1.5V and 2.5V FETs (1.5V as option, 2.5V as base)
  - 3-7 levels of metal (4 µm Al last metal)

- **Wafer**: SOI with 145 nm top silicon layer, 1 µm BOX on 1000 ohm-cm high resistivity silicon substrate to minimize the capacitive coupling to substrate

- Provides a base technology for RF switch designs for various wireless applications

- Competitive cost and performance solution to GaAs pHEMT and SOS technologies
Interweaving opto-electronic devices in a potential low cost production silicon process platform

Realization of photonic functions next to CMOS transistors enables
- More functions in complex electro-optical integrated systems
- Improvement of photonic functions (or imperfections)

Utilize photonics to enhance the performance of electronic IC
- On-chip or chip-to-chip optical interconnects
- Optical delays for radio-frequency filters, phased arrays, etc.

Photonic device fabrication in 7RFSOI
- Passive components (waveguides, delay lines, Y-junctions, couplers, grating couplers)
- Active component
  - Forward and reversed biased p-n traveling wave and ring modulators
  - Thermal modulators
  - Photodiodes: on-chip metal-silicon, off-chip (packaging)
Monolithic 8 x 8 OPA Transceiver

- 180 nm GF 7RF SOI CMOS process
- Over 300 distinct optical components
- Over 74,000 distinct electrical components
- Optical Phased Array (OPA) consists of 64 optical variable thermo-optical tunable phase shifters, attenuators, nano-antennas

By choosing MOSIS as their partner, customers speed their route to commercialization via:

- **Access to broad range of production services**
  - MPWs -> Low Volume Production (50-500+ wafers)
  - Foundry/Test/Packaging + can leverage network of IP/Design partners

- **Expert interface to manage the business transactions**
  - NDAs/Design Kits/Invoices/shipping etc

- **Strong technical support**
  - Over 30 years of experience (60,000 designs managed)
  - Can provide direct answers to 98% of technical questions

- **Close working relationship with imec**
  - Regular review meetings (e.g., quickly resolve technical issues)